JOINT ADVANCED STRIKE TECHNOLOGY PROGRAM

AVIONICS ARCHITECTURE DEFINITION

VERSION 1.0

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EXECUTIVE SUMMARY

This document contains Version 1.0 of the Joint Advanced Strike Technology (JAST) Avionics Architecture Definition. It will be used in the development and demonstration of a set of matured technologies and modular avionics functions to be used in Engineering and Manufacturing Development (EMD) of next-generation strike weapons systems for the Navy, Marine Corps, Air Force and allied nations. The purpose of the Architecture Definition is twofold: (1) to provide a basis for planning risk reduction demonstrations, analyses, and modeling efforts, and (2) when mature and complete, to establish a framework for the consistent application of avionics building blocks to meet the needs of specific platforms. The architecture describes digital hardware modules and components, the system software definition and its design and support environment, the system interconnects, the sensor functions, the electrical power distribution approach, and mechanical aspects of the avionics including packaging and thermal management.

A systematic process has been put in place to develop and update the Architecture Definition. A select group of avionics experts has been assembled from Navy and Air Force organizations to form an Integrated Product Team (IPT). Using the best information available on current and projected avionics technology and on the goals of the JAST program, with especially heavy emphasis on affordability, the IPT developed Version 0.0 of the Architecture Definition as a vehicle to initiate a dialog with the avionics community in both government and industry. The initial version was widely circulated, and extensive written and oral critiques were received. An architecture review board, with extensive industry participation, performed an issue definition and adjudication process with the goal of bringing Version 0.0 to the level of maturity needed to support near term JAST avionics development efforts.

As a result of this adjudication process, the original document has been extensively revised, and a new direction for the maturation and demonstration of JAST avionics concepts has been adopted. The process will be event-driven, with need dates for closure of the remaining avionics issues chosen on the basis of availability of information and of the timing of follow-on activities which depend on decision outcomes. The basic features of the Version 0.0 architecture were maintained, but the revised document is more open in that a wider range of alternative solutions for individual areas of the architecture will be tracked and evaluated up to the point where a decision is needed. In many areas, a leading candidate and a set of tracked alternatives have been identified. Every attempt has been made to incorporate the full spectrum of valid contenders for such areas as sensor integration, system interconnect, and power distribution, recognizing that fiscal and schedule constraints will set limits on the scope of investigation of alternative approaches. Furthermore, the JAST Program will maintain a continuing interaction with industry and government as the Architecture Definition matures and as issues are resolved to ensure that all pertinent information is incorporated and that industry is fully prepared for the start of EMD. Facilitating this interaction are: expansion of the Avionics IPT membership to include the weapons system concept contractors and industry associations representatives, normal interchange as part of JAST contractual efforts, the creation of an Avionics electronic bulletin board, and periodic "Industry Day" briefings.

This Architecture Definition supports the JAST Avionics concept development/demonstration program whose goal is to establish the basis for development in EMD of low risk, affordable avionics suites for a variety of strike weapon systems. This effort is tightly coupled to the overall JAST weapon system concept development and demonstration. Among the products which the JAST program will make available to EMD program managers are:

- Results of a series of risk reduction demonstrations (RRDs) and Integrated Technology Demonstrations focused on specific technical and cost issues;

- Results produced by an end-to-end virtual avionics prototype, including pilot-in-the-loop simulations, to validate the operational suitability of avionics suites with a range of functions and capabilities. The VAP supports the development of the overall JAST weapon system concept. It reflects functional allocations

from the Strategy-to-Task-to-Technology process and provides information on the capabilities and costs of alternative avionics concepts to the weapon system engineering process;

- A set of modular avionics functions, with their associated implementing technologies, which have been reduced to an acceptable level of risk through analysis and demonstration and characterized in terms of cost, performance, and technical maturity for use in EMD. These "building blocks" will include digital information processing hardware and software, a software design and support environment, an information transfer network structure and protocols, sensors and sensor management functions, cockpit/avionics integration, weapons integration and targeting, electrical power distribution, and mechanical aspects of avionics, including packaging and thermal management techniques; and

- An avionics architecture standard which will serve as a framework for tailoring an avionics suite which employs these building blocks and is optimized in terms of cost and performance for any given platform. The architecture will be based on a form/fit/interface (F^2I) approach and will include design rules and implementing standards which comprise a set of "building codes" for avionics suites based on JAST avionics building blocks.

The point of departure for the JAST Avionics Architecture Definition was the Joint Integrated Avionics Working Group (JIAWG)/F-22 Advanced Avionics Architecture. This starting point was chosen because it represents the most recent avionics development in DoD. A description of the F-22 avionics suite is given in Annex A. That baseline has been enhanced in the JAST architecture to take advantage of technology and system concepts which have emerged in recent years. The JAST baseline is thus appropriate for an aircraft which will enter EMD in FY 2000 with an Initial Operational Capability date of 2010. The JAST baseline also supports the primary JAST goal of reducing life cycle cost (LCC) and of supporting a variety of weapon system platforms with a common inventory of technologies and modular functional capabilities.

Key features of the JAST avionics architecture, as described in detail in this document, include the following:

- Emphasis on affordability, open systems adaptability, scalability, incorporation of commercial technology and products, technology independence and growth provisions, and support for high levels of reliability, maintainability, supportability, and deployability;

- Use of an advanced unified digital interconnect scheme;

- Infrastructure which provides efficient, reliable power distribution, environmentally tolerant packaging, reliable connection for electrical and optical signals, and cooling for high intrinsic reliability of electronic devices;

- Extensive support for built-in test and fault isolation, reconfigurability for failure management, and maintenance support;

- Use of an advanced information architecture, supported by a partitioned software architecture, open system-compliant processing hardware, and a mature software engineering environment and methodology;

- Support for commonality, interoperability, and affordable long-term insertion of emerging technology;

- Integrated sensor functions, including sensor management and multifunction apertures; and

- Advanced information management, including fusion of on-board and off-board data sources, support for target recognition and precision targeting, and support for high levels of aircrew situational awareness.

This Architecture Definition is the basic member of a family of documents which collectively describe the JAST avionics architecture and the program through which the avionics concept will be developed and demonstrated. The companion documents, which should be used in conjunction with the definition document to obtain a complete picture of JAST avionics activities, are:

- The JAST Avionics Concept Development/Demonstration Plan (JACDDP) which describes the sequence of studies, demonstrations, and simulation and modeling efforts that will provide the data to refine and validate the avionics concept and the architecture;

- An Issues/Decision/Rationale Document which contains a full description of issues, alternatives, decisions, rationale and a record of issue closures;

- An Annex Document with descriptions of F-22 avionics and other programs which provide support to JAST; and

- An Appendix Document which describes significant technology, standardization, and other programs which have contributed to the enhancement of the F-22 baseline in defining the initial JAST architecture.

Updated versions of the JAST Avionics Architecture Definition will be published with the completion of significant milestones, when essential data becomes available, and as event-driven decisions are made. The release of next version is planned for 3QFY96, although an interim update may be necessary. Comments and relevant information are welcome from all knowledgeable parties. The dialog which has been established, and which proved effective in migrating Version 0.0 to Version 1.0, will be maintained through all available channels, including widespread electronic distribution of this and related documents. Table 0-1 summarizes the primary areas now under consideration, including the corresponding approach in the F-22 point of departure, the leading and other alternatives, and the date by which a decision is required (D-Date) to support subsequent activities.

The Architecture IPT wishes to express gratitude to the industry and government participants whose extensive work and cooperative attitude were essential to the timely completion of this document.

Table 0-1 JAST Avionics Architecture Candidate Standards ("Building Blocks")

F-22 (JIAWG) Point of Departure	JAST Leading Alternative	JAST Tracked Alternatives	D-Date
MECHANICA	**MECHANICAL**		
• SEM-E Format	• SEM-E Format	• Larger, Ease of Manufac.	• Mar 97
• Liquid Flow Thru Cooling	• Liquid Flow Thru Cooling	• Conduct., Air Flow Thru	• Mar 97
• Conduct. Cooling (VMS)	• Conduct. Cooling (VMS)	• Liquid Flow Thru	• Mar 97
• Bendix Connector	• Bendix Connector	• Smaller Connectors	• Mar 97
ELECTRICAL	**ELECTRICAL**		
• 270V Prime Power	• 270V Prime Power	• 115/230V 400/800-1600 Hz	• Mar 97
• 5V Power Thru Bkplane	• 48V Power Thru Bkplane	• 28/270V, (5V, 3.3V, +-15V)	• Mar 97
INTERCONNECTS (N/W)	**INTERCONNECTS (N/W)**		
• Interconnects/ buses (Pi, TM, DFN, HSDB) & FOTR	• Unified Network Protocol (SCI)	• Multiple Interconnects (F-22, Fibre Chan., ATM)	• Mar 96
PROCESSORS	**PROCESSORS**		
• Many Processor Types	• Few Processor Types	• App. Specific Processors	• Mar 97
SENSORS	**SENSORS**		
• Dedicated Apertures	• Integrated Apertures	• Wideband Rx, Narrow Tx	• Dec 97
• Dedicated RF Electronics	• Time-Shared RF Mod.	• F-22 RF Electronics	• Dec 97
SOFTWARE	**SOFTWARE**		
• Op Sys, Sys Mgt (Propr.)	• POSIX (Commercial)	• F-22,Commercial Dev.	• Mar 96
• Ada 83	• Ada 9X	• C / C++	• Mar 96
• Graphics I/F (Custom)	• X-11/Motif	• X-Windows, GKS, PHIGS	• Mar 96

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JAST AVIONICS ARCHITECTURE DEFINITION ISSUES/DECISIONS/RATIONALE DOCUMENT

Notes:
1. Appendices, Annexes, and the Issues/Decision/Rationale Documents are published under separate covers.
2. Annexes are unchanged per Industry/Government review. Comments received in the annexes have been reflected in Version 1.0 of the Avionics Architecture Definition Document.

1.0 Introduction

The JAST Program is chartered to facilitate evolution of fully developed and validated operational requirements, proven operational concepts, and mature demonstrated technologies to support successful development and production of next generation strike weapon systems for the U.S. Air Force, Navy, Marine Corps, and our allies. To support this charter, the Avionics Integrated Product Team (IPT) has the responsibility to develop and demonstrate an affordable avionics "building block" of matured technologies ready for low-risk transition for a 1 October 1999 entry into the Engineering and Manufacturing Development (EMD) phase for a next generation strike weapon system. Essential to this process is the early formation of an infrastructure—the JAST avionics architecture—upon which the avionics building block will evolve. This document, the Avionics Architecture Definition, describes the architecture and facilitates avionics evolution by: (1) providing a basis for planning risk reduction demonstrations, analyses, and modeling efforts, and (2) when mature and complete, establishing a framework for the consistent application of avionics building blocks to meet the needs of specific platforms. The architecture—the "building codes" of avionics—describes digital hardware modules and components, the system software definition and its design and support environment, the system interconnects, the sensor functions, the electrical power distribution approach, and mechanical aspects of the avionics including packaging and thermal management. This section describes the process used to develop the architecture, how it ties into the overall JAST Avionics efforts, the salient points of its current form, and future plans for its evolution.

A systematic process has been used to develop and update the Architecture Definition. An integrated product team (IPT) of Air Force and Navy engineers and scientists developed the JAST avionics baseline using the F-22 EMD avionics as a point of departure (largely because it represents the most recent approach to avionics development in the DoD), and incorporating appropriate enhancements offered by newer technologies. The criteria by which these enhancements "earned their way onto the architecture" were applicability to JAST and its range of strike aircraft requirements, lower life cycle costs, and a maturation path which would ensure a low risk transition of that technology to EMD. Version 0.0 described this baseline and was released on 5 June 1994 to industry, government, and academia for review and comment (over 100 organizations reviewed the document). The Architecture IPT, expanded in membership to include weapon system concept contractors and industry associations representatives, then convened an adjudication review board over a four-week period. This IPT, along with several additional invited architecture experts in the field of avionics, reviewed and discussed the over 650 comments received. This version reflects the results of that review process. The comments were wide and varied. Many influenced the standards; some even influenced the architecture definition strategy itself.

For example, in response to a consistent comment that the Version 0.0 standards prematurely drove to a point solution which had not "earned its way onto the architecture," the Architecture IPT refocused the Definition process to follow a more event-driven strategy. Based on the JAST goals of affordable avionics capable of meeting a range of strike requirements in the 2010 to 2040 timeframe, the state of technology and it projections for the future, and the Avionics maturation plan, the board identified the viable candidates for each standard, where applicable, and determined the "need date" to reach a downselect decision. This procedure not only permits near-term design trade flexibility and avoids premature "lock-in" of standards which may later become inappropriate, but it also bounds the architecture framework and ensures that the architecture evolves with the appropriate definition to support the avionics building block and the overall weapon system concept development. [The decision dates are tied to specific events identified in the JAST Avionics concept development and demonstration plan. The plan, published under separate cover, offers the latest description of the sequence of studies, demonstrations, and simulation and modeling efforts that will provide the data to refine and validate the avionics concept and the architecture.]

Because of schedule and resources constraints, the review board divided the standards candidates into leading and tracked alternatives. The leading candidates, based on the data available to date, best complied with the JAST architecture guidelines (see Section 2). The alternative candidates offer both a feasible competitor as well as a potential fall-back solution to the leading candidate. All candidates, including the leading candidate, must earn

their way onto the architecture as a result of life cycle cost analysis, and demonstrated results. During the period leading up to the downselect decision dates, a combination of data review, trade studies, and demonstrations will be used to determine the appropriate standard to use. Concurrent to these evaluations will be avionics risk reduction, concept development, and demonstration activities supporting the weapon system concept and a 1 Oct 99 Milestone II decision. Thus, the process used to develop the architecture both drives and responds to the other Avionics activities.

This Architecture Definition supports the overall JAST Avionics effort: it is the basic member of a family of documents which collectively describe the JAST avionics architecture and the program through which the avionics concept will be developed and demonstrated. The companion documents (each published under separate cover), which should be used in conjunction with the definition document to obtain a complete picture of JAST avionics activities, are:

- The JAST Concept Development and Demonstration Plan which describes the sequence of studies, demonstrations, and simulation and modeling efforts that will provide the data to refine and validate the avionics concept and the architecture;

- An Issues/Decision/Rationale Document which contains a full description of issues, alternatives, decisions, and decision rationale and a record of issue closures—in essence, a traceability document for decisions made today which affect activities later in the program;

- An Annex Document describing the F-22 avionics and Airborne Shared Aperture Program—useful information that provide both support and reference for JAST avionics concept development; and

- An Appendix Document which describes significant technology, standardization, and other programs which have contributed to the enhancement of the F-22 baseline in defining the initial JAST architecture.

In its current form, the Architecture Definition contains the following salient points or features:

- Emphasis on affordability, open systems adaptability, scalability, incorporation of commercial technology and products, technology independence and growth provisions, and support for high levels of reliability, maintainability, supportability, and deployability;

- Use of an advanced unified digital interconnect scheme;

- Infrastructure which provides efficient, reliable power distribution, environmentally tolerant packaging, reliable connection for electrical and optical signals, and cooling for high intrinsic reliability of electronic devices;

- Extensive support for built-in test and fault isolation, reconfigurability for failure management, and maintenance support;

- Use of an advanced information architecture, supported by a partitioned software architecture, open system-compliant processing hardware, and a mature software engineering environment and methodology;

- Support for commonality, interoperability, and affordable long-term insertion of emerging technology;

- Integrated sensor functions, including sensor management and multifunction apertures; and

- Advanced information management, including fusion of on-board and off-board data sources, support for target recognition and precision targeting, and support for high levels of aircrew situational awareness.

The JAST avionics architecture described in this document assumes a very broad definition of strike avionics characteristics. Specific numbers in terms of operations per second, instructions per second, bits per second, weight, power allocations, source lines of code, etc., are not specified. Instead , this document provides some estimates necessary to scale and bound the problem. This document assumes an open system architecture that will allow the addition and deletion of functionality using a "plug and play" scenario for hardware with unambiguous software interfaces. Proprietary information is minimized and any number of vendors could provide hardware and software that meets the interface standards. Table 0-1 (see Executive Summary) summarizes the primary issues now under consideration, including the corresponding approach in the F-22 point of departure, the leading and other alternatives, and the date by which a decision is required (D-Date) to support subsequent activities.

While Version 1.0 represents the current definition of the JAST avionics architecture, the Architecture Definition is a living document which will evolve over the course of the JACDDP. Various concepts and trade studies for JAST avionics are ongoing and new studies will soon be underway. The mix of on-board and off-board assets that will provide the warfighter with effective mission performance at the lowest cost will be determined and demonstrated over the next few years. These efforts will refine the architecture definition and the avionics contribution to the weapon system concept. Updated versions of the JAST Avionics Architecture Definition will be published with the completion of significant milestones, when essential data becomes available, and as event-driven decisions are made. The release of next version is planned for 3QFY96, although a interim update may be necessary.

Comments and relevant information to Version 1.0 from all knowledgeable parties are welcome. The dialog which has been established, and which proved effective in migrating Version 0.0 to Version 1.0, will be maintained through all available channels, including widespread electronic distribution of this and related documents.

The Architecture IPT wishes to express gratitude to the industry and government participants whose extensive work and cooperative attitude were essential to the timely completion of this document.

[Note: Version 1.0 differs in format from Version 0.0 in three ways. First, changes in the text and tables are indicated by "change bars" in the right-hand margin. Second, several sections now show the applicable standard, the leading and alternative candidates, and the associated downselect decision date. Finally, under separate cover, the "Issues/Decision/Rationale Document" provides a composite picture of the various issues addressed in Version 0.0 and the accompanying industry/government comments. The adjudication board’s decisions and supporting rationale provide both insight and a historical trace of the architecture definition process.]

2.0 JAST Avionics Architecture Guidelines

The Architecture IPT has established the following guidelines for establishing the architecture standards and identifying viable candidates.

2.1 Affordability

Affordability is of primary importance to the JAST. Therefore the JAST avionics architecture must be predominantly driven by cost considerations. The avionics architecture should seek to reduce life cycle costs, especially development costs. Affordability constraints require the architecture to support an open system concept, insertion and use of commercial and openly available military technology/standards, and the reuse of software.

2.2 Scalability

The JAST avionics architecture should be guided by the need to adapt to a wide range of strike mission requirements and systems. The architecture must be able to handle future growth in requirements and different needs among the Navy, Air Force, and Marines. A JAST scalable architecture should emphasize the partitioning and modularity of software and hardware. In addition to modularity, the interconnect system, the power distribution system, and the cooling system must be able to handle increased loads to meet whatever needs arise. Overall, the avionics architecture must meet the need for additional functionality with incremental improvements without disrupting existing performance or compromising needed capability.

2.3 Open System Adaptability

The JAST avionics should promote the use of an open architecture to allow modules built by different vendors to work together and to promote increased competition at the module level. Development costs can be reduced by not relying on proprietary hardware and software. By publishing open system module standards early in the development process vendors are encouraged to seek opportunities and develop modules for areas where they feel they have a competitive edge. Open systems with well-defined standard interfaces create an environment where vendors can compete for specific modules without competing for the entire system.

2.4 Commercial Technology

The JAST architecture should rely heavily on commercial software and hardware technology to control costs. The use of commercial technology reduces the avionics development costs and offers an upgrade path to newer technology as it is developed by commercial industry. This provides a means of attaining the maximum in available performance not only at development time, but also over the life of the aircraft. Commercial software and design environments allow avionics designers and implementors to use more mature (higher quality) tools during the JAST development phase. However, the harsh environment and restraints on weight and volume found in tactical aircraft place restrictions on the amount of commercial technology which can be used.

2.5 Reliability and Supportability

Reliability and supportability are significant features of the JAST avionics. They are significant contributors to overall aircraft availability in both peacetime and wartime. Aircraft availability impacts the total number of aircraft required, and hence the cost, for a given combat capability. Aircraft unavailable because of malfunctioning avionics make no contribution to the war fighting capability.

Avionics reliability and availability have a large impact on the size (and hence the cost) of the maintenance "tail". If the aircraft has a high reliability and availability, it may be possible to fight the early days of a war without avionics maintenance capability. This may be particularly important for ground based aircraft such as the AF uses, because maintenance personnel and equipment must often be deployed to newly established remote bases.

The JAST avionics should continue to operate in the presence of data/timing errors, failed hardware modules, and software errors. Accordingly, fault-tolerance and integrated diagnostics are important considerations in meeting the reliability and supportability constraints. However, the amount of redundant avionics components which can be economically carried to provide this capability must be carefully evaluated. Too little redundancy will result in an aircraft with low availability. Too much redundancy will result in an overly large and costly aircraft. Moreover, the possible need to fight the early days of a war without a maintenance capability can affect the required level of redundancy.

Fault tolerance and integrated diagnostics support in commercial module designs may not be as extensive as that desired for military applications. Joint Test Action Group (JTAG) and other test provisions are becoming more prevalent, but commercial vendors do not generally dedicate sufficient resources to test and diagnostics needed to meet military requirements. This limitation will be considered when making decisions about the use of commercial components.

The JAST avionics architecture should support a reduced maintenance concept. Repair level analysis and LCC analyses will be performed to determine the most cost effective maintenance concept that meets user requirements. As a minimum, the architecture should support two-level maintenance and in some cases, one level maintenance or throw away modules.

The JAST avionics architecture maintainability requirements will be based on the most stringent Navy, Air Force, and Marine requirements. In the case of the Navy, for example, the carrier has limited flight deck space in which any repairs or maintenance can be performed. In addition, it is a harsh environment for opening up aircraft. Carrier decks host high intensity electro-magnetic fields that can potentially damage the exposed electronics. Moreover, spills from fluids onto a steel deck are of concern to the Navy.

A paperless data flow, continuous from on-aircraft fault data storage to organizational repair data to depot level module repair should be encouraged. There should be a standardized electronic format established for the transfer of maintenance and BIT data. This will aid in the reduction of can-not-duplicate (CND) discrepancies.

Other advanced reliability and supportability concepts should be considered for the JAST avionics architecture. For example, paperless technical orders, on-module storage of module status and fault data, and integrated diagnostics, among others, can influence the affordability and LCC of JAST avionics.

2.6 Technology Independence and Growth

The JAST avionics architecture should minimize the reliance on specific technology implementations. The architecture should emphasize well defined interfaces, communication protocols, and software modularization that allows it to evolve over time. Target hardware and software should be upgradable without causing a need for a massive redesign. In addition, the number and need for specialized processors should be minimized by the architecture.

2.7 Data Rate and Throughput Guidelines

Table 2.7-1 contains the projected data rate and throughput for various electro-optical (EO), radar, electronic warfare (EW), and communication, navigation, and identification (CNI) applications. These data have been provided by various government sources, along with contractor inputs during the Version 1.0 adjudication process. Overall, the projected data rate for a JAST 2010 EO system is 120 - 700 Mbits/sec per channel and 15 - 25 GOPS for throughput. A JAST 2010 radar system is projected to require an estimated data rate of 200 - 800 Mbits/sec per channel and a throughput of 2 - 15 GOPS. A JAST 2010 EW suite is projected to require an estimated data rate per channel of 0.05 - 2.0 Gbits/sec and 1 -3 GOPS throughput (exclusive of the EO fraction carried above). CNI throughput is projected at 30 - 50 GOPS, but most of this is typically done by specialized preprocessors.

The numbers given in the Table 2.7-1 assume that the given function will be included in the aircraft sensor or processing suite. This may not be the case. Off-board sensors may replace some of the functions listed. Therefore, the numbers given are only an estimate of what may be required if the function/sensor listed is on-board.

The data rates given in the table 2.7-1 are for unbuffered data rates. The ADAS data rate is an aggregate data rate of multiple sensors.

The processing throughput requirements are based on the "to be delivered" throughput as opposed to the "specified processor" throughput. This is an important distinction since the specified processor throughput will be higher than the “to be delivered” throughput based on the processor efficiency. For example, if a processor is capable of achieving 50% throughput for a given application and the required delivered throughput is 9 GFLOPS, then the specified processor throughput will need to be at least 18 GFLOPS. Experiences have been that it is possible to have processor efficiencies less than 50%, therefore, the required specified throughputs are driven up even more drastically than the example.

Table 2.7-1 Data Rate And Throughput Projections

Application (Year 2010)	Data Rate Projection (per channel)	Throughput Projection (includes preprocessing)
IRST	120 - 200 Mbits/sec	4 - 10 GOPS
FLIR	120 - 160 Mbits/sec	3 - 10 GOPS
ADAS		
SIT Awareness	150 - 700 Mbits/sec	4 - 10 GOPS
Navigation	150 - 700 Mbits/sec	1 - 2 GOPS
Threat Warning	150 - 700 Mbits/sec	1 - 4 GOPS
RGHPRF	280 Mbits/sec	
ASLC + RGHPRF	280 Mbit/sec	2-15 GOPS
SAR	200-800 Mbits	
EW-RF (RWR/ESM)	1 -2 Gbits/sec	0.5 - 2.0 GOPS
EW-EO (Missile Warning)	SEE ADAS ABOVE	SEE ADAS ABOVE
EW-C3 (Special Receiver)	200 - 400 Mbits/sec	0.5 - 1.0 GOPS
EW-EO (Laser Warning)	50 - 100 Mbits/sec	50 - 100 MIPS
Total EO		15-25 GOPS
Total Radar		2-15 GOPS
Total EW suite		5 - 11 GOPS
Total CNI suite (WBDL+GPS+IFF)	TBD	30 - 50 GOPS*

* Normally done by specialized preprocessors

2.7.1 Application Definitions

Infra-Red Search and Track (IRST): EO function used in an offensive situation and includes both spatial and temporal processing. Will be either a stand-alone function or a simultaneous function with either Automatic Target Recognition (ATR) or an Advanced Distributed Aperture System (ADAS).

Forward Looking Infra-Red (FLIR): EO function used for targeting. Will be either a stand-alone function or a simultaneous function with either ATR or ADAS.

Advanced Distributed Aperture System (ADAS): EO function used for pilot night vision situation awareness for either: (a) IR threat warning for short-range ground to air missiles or (b) for defensive IRST against long-range air-to-air targets or ground-to-air missiles. The ADAS is a multi-sensor configuration in which sensors are distributed on the skin of the aircraft. The data rate given in the table is an aggregate of the total sensor data rate.

Range-Gated High Pulse Repetition Frequency (RGHPRF): Radar function used for an all aspect (nose and tail) air-to-air waveform.

Adaptive Side Lobe Cancellation (ASLC): Radar function used for the cancellation of side lobes. This function would be used simultaneously with the RGHPRF.

Synthetic Aperture Radar (SAR): Air-to-ground radar function used for image ground targets.

Electronic Warfare - Radar Frequency (EW-RF): Radar warning receiver (RWR) function and electronic support measures (ESM) function for electronic countermeasures will be combined with the data rate and throughput projections given for a 500 Mhz instantaneous bandwidth channel with multiple high-speed analog to digital converters. Additional instantaneous bandwidth requires additional channels.

Electronic Warfare (EW-EO & C3): Passive missile warning, laser warning, and special receiver functions are all aspect (multi-apertures) and include multi-spectral, spatial, and temporal processing. Missile warning will be either a stand-alone function or combined with other EO sensors given above.

Communication, Navigation, and Identification (CNI) Suite: CNI functions include wideband data link, GPS, and IFF. The throughput projection includes preprocessing.

3.0 JAST Architecture

The JAST architecture is based on the definition of overall system concepts and identification of interfaces and "building codes". These building codes include the specification of digital interfaces, module mechanical format (including cooling and module size), power, backplane, and other interconnects, and software using the guidelines outlined in Section 2.0. Advances in technology gained through the Air Force PAVE PACE program, the Navy Advanced Avionics Subsystems and Technologies (AAST), and the Next Generation Computer Resources (NGCR) programs, as well as others, have been leveraged to reduce risks and LCC in defining this architecture.

The key features of this architecture are as follows:

- Commercial technology will be exploited to the maximum extent possible consistent with tactical aircraft requirements.

- A unified avionics network protocol is proposed to replace numerous types of aircraft-internal networks. This advanced network is expected to result in cost and weight savings due to decreased module input/output (I/O) pin count, fewer gateway modules, and the capability to locate processing resources anywhere in the aircraft, as well as supporting simplified control software.

- A robust architecture allows for cost savings through the sharing of resources and the flexible use of off-board assets to allow an austere platform to be used for a variety of missions.

- Leveraging the module mechanical and cooling technology from the F-22 is proposed to provide low risk approach, to reduce costs through economies of scale and to provide retrofit for the F-22.

- Software interfaces across the application to operating system boundaries are proposed to use POSIX/Ada 9X bindings in such a way as to break hardware/software dependencies. As a result, software should be more easily reused within and across weapon systems, resulting in cost savings.

- Integrated RF support electronics are proposed as a major cost savings through resource sharing. Further, the unified network approach allows the extensive use of BIT and system reconfiguration at the module level for both digital and RF hardware. A savings in maintenance and manpower costs is expected to result.

- Shared RF apertures are proposed to the extent which they reduce cost for the capability needed. Since the JAST program anticipates the extensive use of off-board sensors, the need for sharing apertures across functions may be minimized.

- An integrated EO subsystem is proposed to achieve affordability, mission needs, and reduce aircraft signature. Again, the extensive use of off-board sensors may reduce the need for integrating EO subsystems.

The JAST architecture, as shown in Figure 3.0-1, is based on the PAVE PACE architecture which has been identified as an appropriate evolution of the F-22 point-of-departure architecture. An overview of the PAVE PACE architecture is provided in Appendix B. The architecture consists of an integrated core processing subsystem, an integrated RF sensing subsystem, shared RF apertures, an integrated EO sensing subsystem, a stores management system, a vehicle management system, and a pilot vehicle interface, as well as the interconnects among them. The unified digital avionics network provides the interconnect between the integrated core processor, the sensing functions, the vehicle management system (VMS), and the pilot vehicle interface.

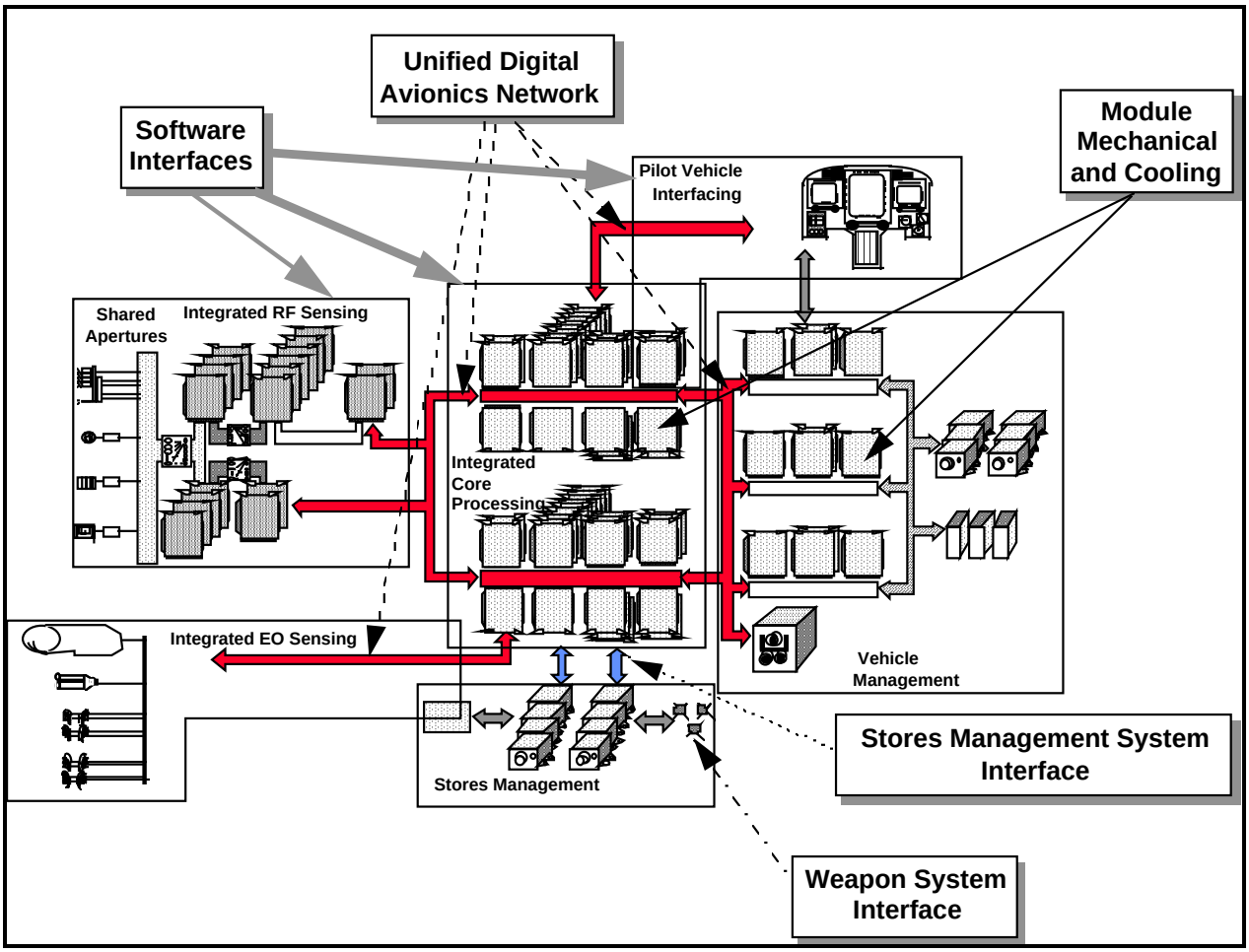

Figure 3.1 JAST Advanced Architecture Showing Interface Standardization Areas

3.1 Use of Commercial Technology

A prime tenet of the JAST architecture is to reduce costs by using commercial technology to the greatest extent possible. Use of commercial technology is most possible and most desirable in the digital area where the commercial computer industry is making giant strides yearly. In the analog area, while commercial industry is still moving rapidly, many of the developments are not as directly applicable to the military as in the digital area. For example, in the area of RF circuits, the DoD is finding it necessary to fund the Microwave/Millimeter-wave Monolithic Integrated Circuit (MIMIC) program while in the area of digital circuits development is moving ahead without DoD funding. In the area of sensor and aperture development, the DoD is the leader. As a result, the commercial sector is leveraging DoD technology more than DoD leverages commercial technology. However, there are still instances in the analog circuitry area and the sensor area where commercial and military technology overlap and commercial technology or manufacturing can be leveraged.

Figure 3.1-1 shows a spectrum of use of commercial digital hardware and software technology in military systems. While some military systems (such as the Navy Tactical Advanced Computer used on ships) have been successful in working at the right hand side of the hardware and software spectra shown below, tactical aircraft have traditionally been closer to the left hand side. Digital hardware environments have required high temperature Integrated Circuits (ICs) in hermetic packages and mounted on boards able to withstand extreme vibration. However, JAST is seeking to move more toward the right of the spectrum.

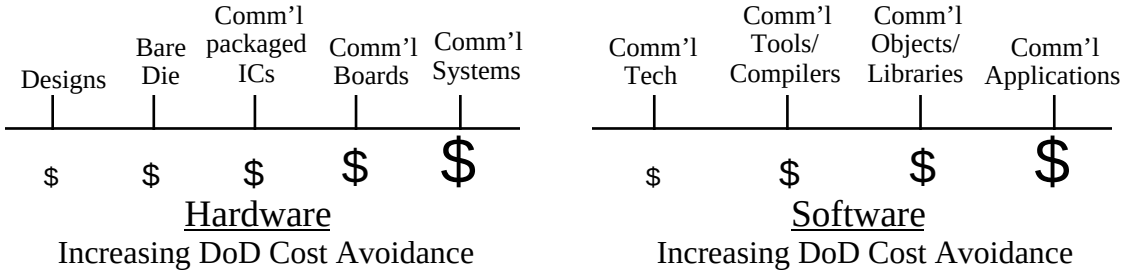

Figure 3.1-1. Spectrum of Using Commercial Technology

In particular, the JAST architecture provides for leveraging commercial designs for computer data processing CPUs, for signal processing central processing units (CPUs), for memories, and for support circuitry. It also allows for using "mil-spec" versions of commercial computers including parallel processors. This permits support software and operating systems to be moved with relatively little modification directly from commercial systems to the JAST architecture. The areas where modification may be necessary are real time support, fault tolerance, security, and built-in-test (BIT). The recent DoD Directive to utilize commercial products to the maximum extent practicable will result in up-front studies to determine the extent to which the technology can be affordable used.

3.2 Standards Only At The Interfaces

Another basic tenet of the JAST architecture is that standards are specified only at the module interface level. This is sometimes termed a form, fit, interface (F^2I) approach rather than the form, fit, function, interface (F^3I) approach which was proposed for JIAWG avionics. The F^2I approach has been used by the Navy NGCR program. With it no attempt is made to standardize what functions a module performs nor how it performs them. It is left to the module developer to determine what goes into the module as a function of life cycle cost considerations. The use of a standard application program interface (API) and programming in a high order language such as Ada may alleviate the need to specify a particular instruction set architecture. However, these benefits need to be weighed against the supportability issues incurred with multiple ISAs. It is recommended that the decision of whether or not to specify a particular ISA, or family of processors, be left to the EMD teams and that the decision be one of affordability.

3.3 Advanced Unified Digital Interconnect

Standard:	Interconnect
Goal:	A unified digital interconnect protocol covering all digital interconnects
Leading Candidate:	IEEE Std 1596-1992, IEEE Standard for Scalable Coherent Interface (to be used un SCI/RT is available)
Other Candidates:	F-22 interconnects, Fibre Channel, ATM, Custom interconnects
Decision Date:	March 1996

An advanced unified digital avionics interconnect protocol is planned for the JAST architecture. Advances in technology since the mid 1980s have produced new commercial interconnects with speeds an order of magnitude higher than those currently used in our most advanced aircraft--although these networks are yet to be proven in tactical aircraft. The speed and flexibility of these new interconnects opens the opportunity for reducing JAST avionics costs by allowing a single interconnect protocol to replace most or all of the interconnects in our current advanced aircraft. Figure 3.3-1 shows a typical integrated avionics system with a single unified interconnect performing the functions of a variety of, what have been, separate interconnects. For example, in the case of an F-22 like architecture the unified interconnect could replace the Parallel Interconnect (PI)-Bus, the Data Network (DN), the Test and Maintenance (TM)-Bus, the High Speed Data Bus (HSDB), and the sensor/ video/ inter-rack connection.

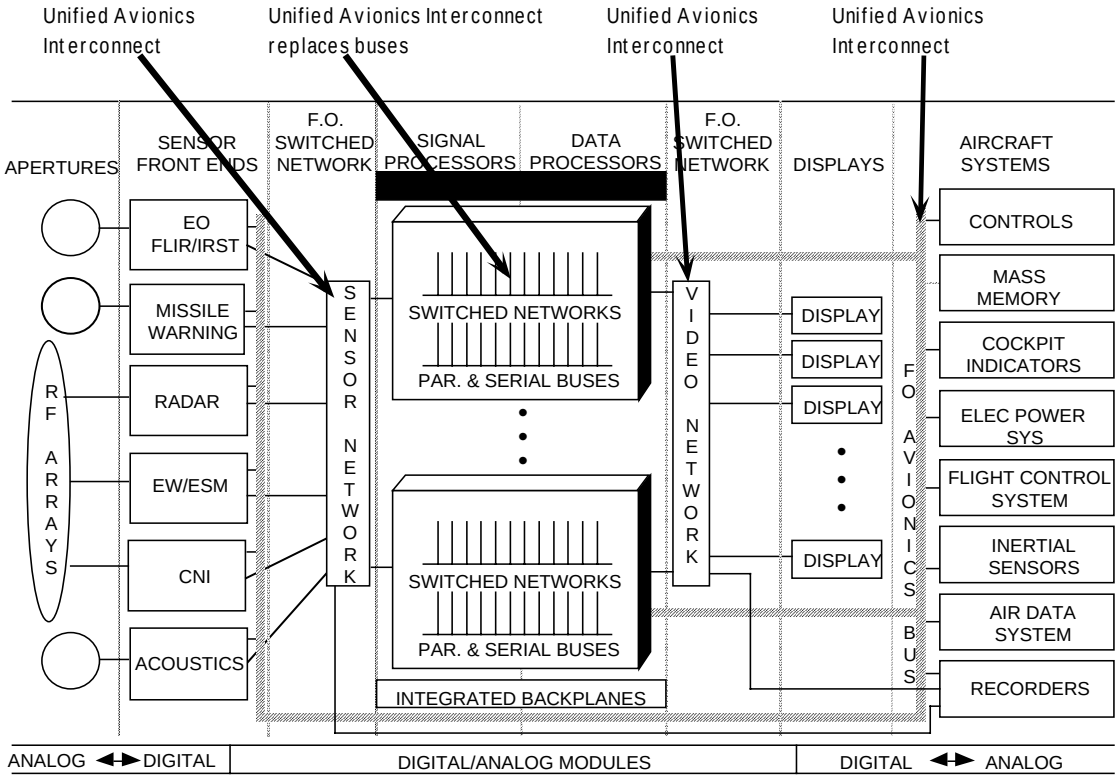

Figure 3.3-1
An Avionics System with a Single Unified Network Protocol Replacing Several Different Current Interconnects

3.3.1 Characteristics Required of A Unified Interconnect Protocol

The general characteristics sought in a unified interconnect protocol are that it have high speed, low latency, support for both message passing and shared memory computing paradigms, scalability from small to

large systems, support for a serial, or low pin-count parallel, instantiation, support for both distributed and centralized switches, support for both electrical and optical physical layers, relative insensitivity to distance, fault tolerance, support for real time computing, and low cost.

High throughput is needed for high bandwidth sensors, and the bandwidth needed to interconnect sensors will increase as analog to digital (A/D) converters increase in speed. Work is going forward on all-digital RF systems in the lower frequency range allowing the carrier frequency to be sampled directly (with extremely fast A/D converters). Experiments are being conducted with optical and other technologies applied to A/D converters which will result in sampling in the giga samples per second range and network requirements in the giga-byte per second range.

High throughput is also needed for inter-processor communications. For example, shared memory systems require extremely high bandwidth (and low latency) interconnects. Shared memory type processors hold promise for applying commercial parallel processor and supercomputer technology to computationally intensive avionics problems. Supercomputer technology has the advantage that its applications software is quite transportable and easily scales upward allowing it to be moved to newer technology hardware with minimal change. Applying this technology would also allow leveraging of the large commercial investment in parallel processor and supercomputer software. In addition, high throughput interconnects simplify even message passing systems by eliminating the necessity for programmers to optimize software to reduce message traffic.

Low latency is needed particularly by shared memory systems, but also by message passing systems which use the same network for command and control as for data flow--as is required for the unified interconnect protocol. In shared memory applications, even cache coherent ones, very high speed (300 Mhz and up) processors may be stalled for hundreds of cycles if the network has high latency. In message passing systems, high latency interconnects often result in very low efficiency parallel processors. Recent experiments in commercial message passing parallel processor systems have demonstrated that even moderately high latency interconnects can have a devastating effect on processor efficiency.

Scalability of the interconnect is needed to allow addition of the numerous new functions which will be required through the thirty years, or more, life of the aircraft. It is also needed to allow insertion of new higher performance technology which will undoubtedly be developed during this thirty plus years. A scalable interconnect protocol provides a low cost interconnection for low performance systems while growing in bandwidth for high performance systems. Serial, or low pin count parallel, interconnects are required to reduce the complexity of the backplane and to reduce the vulnerability of the system to connector contact failure. Both distributed and centralized switch support is needed to accommodate the wide range of design space required to provide the optimum solution for different computational functions. Figures 3.3.2-1 through 3.3.2-5 show some of the many different designs which the interconnect needs to support.

Electrical and optical physical layers are needed to meet the range of requirements a unified network must support. Electrical implementations are cheapest (at this point in time) and generally suitable for module to module communications inside a rack. Optical interconnects are immune to EMI and can travel long distances. Rack to rack and sensor to rack interconnects are likely to be optical. Distance insensitivity in the interconnect allows computing devices to be placed in the aircraft wherever it is most convenient for maintenance access, for weight balance, or for other reasons. It also allows the same interconnect to be used for sensor-to-rack and rack-to-rack interconnect as well as module-to-module interconnect. The general level of fault tolerance required of the interconnect is that failures should have a high probability of detection and that no single failure should take down the entire interconnect (in some cases it may be acceptable to lose a section of the interconnect). Generally this requires a redundant interconnect or some form of error correction.

A real time capability is needed to allow high priority command and control data to be delivered in a timely fashion, even when mixed with large amounts of low priority data. This can be done by using non-shared interconnects (e.g. centralized switch), lightly loaded interconnects, or by some form of scheduling.

Cost effectiveness involves much more than the cost of the interconnect. It includes cost avoidance by being highly scalable for future upgrades as well as cost avoidance by supporting easy-to-program computing paradigms. It also includes cost avoidance (including the aircraft structure multiplier) by eliminating bridge and interface modules.

The leading candidate for the unified interconnect protocol is the IEEE Scalable Coherent Interface (SCI) and its derivative SCI/Real Time (SCI/RT). SCI is an established IEEE commercial standard (IEEE 1596) with integrated circuits (ICs) now available off-the-shelf. SCI/RT is an enhancement to SCI mainly to improve its real time and fault tolerance capabilities. A draft version of SCI/RT standard is now available from the IEEE with some changes still being made. SCI can provide a near-term unified interconnect protocol with a goal of shifting to SCI/RT.

3.3.2 Using a Unified Network for the Test Maintenance Function

Performing the test-maintenance function on a unified network requires attention to some special considerations. To perform the module test function requires a "back door" access to resolve the ambiguous test case where a module does not respond to a query and it is not known if the module or the interconnect failed. Use of dual interconnects on a module can satisfy this need as well as provide fault tolerance when an interconnect fails.

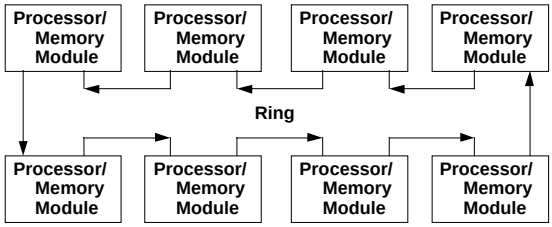

Figure 3.3.2-1 Basic Ring

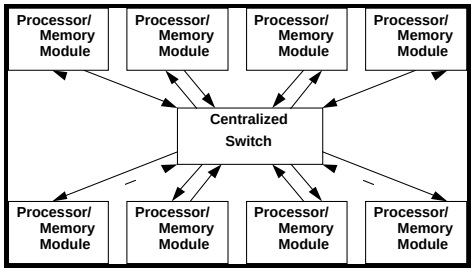

Figure 3.3.2-2 Central Switch Two Party Rings

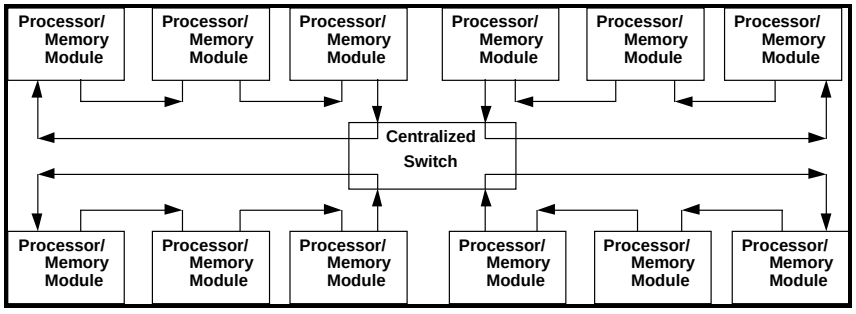

Figure 3.3.2-3 Rings Interconnected by a Switch

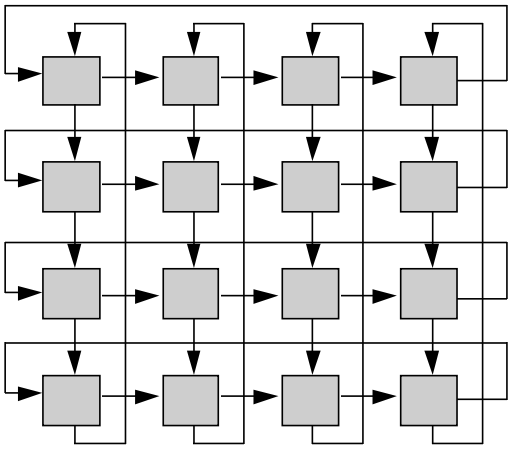

Figure 3.3.2-4 Distributed Switch, Toroidal Mesh Fault Tolerant

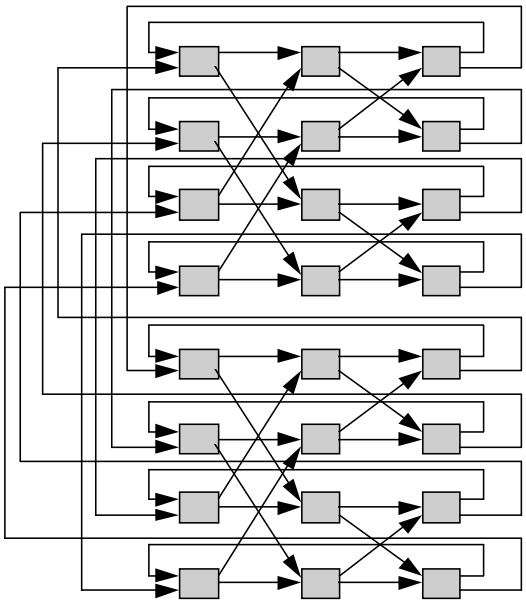

Figure 3.3.2-5 Distributed Switch, Wrapped Butterfly -- Fault Tolerant

3.4 Advanced Electrical Power Description

3.4.1 Aircraft Primary Power

Standard:	Primary Power
Goal:	To choose the optimal primary power for the aircraft and avionics.
Leading Candidate:	F-22-270 VDC
Other Candidates:	115/230V@400 Hz (most current aircraft), 115/230@800-1600 Hz (newer airliners)
Decision Date:	Mar 97

The JAST avionics architecture power distribution system will be supplied by the aircraft's primary electrical power system which will provide either 270 volt DC power, 115/230 volt, 3 phase, 400 Hz power, or 115/230 volt, 3 phase, 800-1600 Hz power. The leading candidate is 270 volt DC, because of extensive F-22 power trade studies, which examined efficiency, cost, weight, volume, and spectral purity requirements of the aircraft. However, additional trades will be made due to the Navy carrier requirements and existing carrier support equipment. In the case of electronically scanned arrays, a 270 VDC to consumption voltage single-stage converter is the preferred concept.

3.4.2 Backplane Power

Standard:	Backplane Power

Goal:	To choose the optimal backplane power for the avionics.
Leading Candidate:	48 VDC as described in IEEE 896.5, Standard for Futurebus+, Profile M (Military), Section 6.4.1 Profile Power
Other Candidates:	28 VDC, 270 VDC, (5 V, 3.3 V, ±15 VDC (analog))
Decision Date:	Mar 97

For integrated racks that may support both digital and analog circuitry, the goal is to use a single backplane distribution voltage of 48 VDC. Small on-module converters would then be used to convert the 48 V to 5 V, 3.3 V, 2.5 V, and lower voltages as needed for digital circuitry. On-module converters would also be used to convert the 48 V to ±15 V or other voltages needed for analog circuitry. This creates a two-stage power conversion system for the integrated racks as opposed to the single-stage conversion used for the sensors. The first stage conversion is done inside the rack by 270 V to 48 V converter modules. The second stage conversion is done on-module by a very small 48 V-to-consumption voltage converter.

The motivation for two-stage conversion and distribution of 48 V through the backplane is to reduce the backplane amperage required for low voltage but high power consumption modules. With the very high density of electronics now being achieved, modules in the power consumption range of 200 Watts are anticipated. In addition, low voltage ICs are being developed for lap top computers and other applications. Currently 3.3 V parts are beginning to be used. In the near future, 2.5 V parts are anticipated. In the more distant future, 1.5 V or 1.25 V ICs are expected. Combining a 200 Watt module with 2.5 V circuitry requires 80 amperes of consumption current. This is too much amperage to be handled by either the backplane connector or the backplane itself. Moreover, because of high frequency switching of on-module circuitry, most amperage is carried on the surface of the conductor. This "skin effect" phenomenon requires that large numbers of power and ground planes be used in the backplane to control the noise. The result is a very heavy and expensive backplane. Increasing the backplane voltage to 48 V solves this problem. However, it does lead to less efficient two-stage power conversion. The intermediate voltage (48 V) was picked because it is in the proper range and because it is an emerging commercial standard used by the telephone industry and others.

In the near term, very small 48 V to consumption voltage power converters for SEM-E modules are not available. However, both the AF and Navy have at various times had programs to further development in this area. Because of this, in the near term, it may be necessary for JAST backplanes to be flexible enough to accept 3.3 V, 5 V and ±15 V as well as 48 V. Modules should have pins reserved on them for these voltages. IEEE 896.5, Standard for Futurebus+, Profile M (Military), Section 6.4.1 Profile Power will act as the guiding document for the JAST backplane power distribution system. However, power and ground pin assignments for the JAST unified network will be made after interconnect trades are performed.

3.5 Module Cooling

Standard:	Module Cooling
Goal:	To establish a mthodology for the avionics modules which ensures adequate reliability of all on-module components
Leading Candidate:	F-22 Liquid Flow Thru Cooling (F-22 Common Module Specification 5PTA3242) for mission avionics F-22 Conduction cooled for the VMS system
Other Candidates:	Conduction cooled, Air flow through cooled, Convection cooled
Decision Date:	March 1997

The preferred cooling concept for mission avionics is liquid-flow-through (LFT) cooling using polyalphaolefin (PAO) as the coolant. LFT has the advantage that it can cool a several-hundred watt module while maintaining even temperature across all ICs on the module. Hot spots are well controlled. LFT allows very high density packaging which in turn reduces the overall weight and size of the airplane. In addition, it keeps the overall module cooler. This decreases module failure rate and increases overall reliability. Another advantage of

LFT is that it may make the use of commercial ICs on military modules more viable by keeping temperature within the 70C ambient specified for those ICs.

The main arguments against LFT are that liquid systems require special maintenance, that PAO spilled on a Navy carrier deck could be hazardous, and that LFT is outside the mainstream of commercial technology and hence expensive.

Other candidate cooling methods are conduction cooling, air flow through cooling, and direct impingement convection cooling. Conduction cooling can handle a maximum load of approximately 50 watts. Air flow through cooling, where air is blown through plenums in the metal core of the module, has a capacity of approximately 90 watts. Convection cooling, where air is blown between modules and directly onto ICs, has a capacity of approximately 100 watts, but is very configuration dependent. It also has the disadvantage that outside air, which may contain corrosive pollutants, is blown directly on the ICs and may reduce reliability. None of the alternative candidates provide the amount of cooling which is provided by LFT.

The preferred cooling concept for the VMS system is conduction cooling. Using conduction cooled modules and an air cooled rack makes the VMS independent of any failures in the liquid cooling system. In addition, VMS modules are generally low performance and have low heat loads. However, it is possible to use dual redundant liquid cooling systems to increase the reliability of LFT. The inherent reliability of conduction cooled boards in an air cooled rack, and F-22 compatibility, were the main reasons for choosing conduction cooling for the VMS system.

3.6 Module Form Factor, Mechanical, and Connector

Standard:	Module Form Factor
Goal:	To establish a unified modular form factor which meets fighter weight, volume, and environmental requirements and is economical to produce.
Leading Candidate:	F-22 SEM-E module
Other Candidates:	VME 6U specification, IEEE 896.5 module size 10SU, new form factor designed for ease of manufacture
Decision Date:	March 1997

The F-22 form factor, mechanical interface, and connector were selected as the JAST preferred concept. The F-22 mission avionics uses a version of the SEM-E format. It is double sided and approximately 6”x6”. The basic pitch is .6”, although some modules are multiples of the .6” pitch. The connector is the Bendix bristle brush which in its basic format has 360 contacts. There are several versions of the connector for use with coax, fiber optics, and on the power supply modules.

The leading candidate for the Vehicle Management System (VMS) is also a version of the SEM-E. It also uses the Bendix connector. However, it is conduction cooled to the card edge for use in air cooled racks.

The rationale for choosing the F-22 SEM-E module format for the mission avionics was primarily to limit the proliferation of different types of liquid flow through (LFT) formats in the DoD. At this time the F-22 LFT format is the dominant form factor. A few other LFT modules have been developed, but the volume of them is far smaller than the volume of the F-22 modules. Moreover, an IEEE standard (P1101.9) is being developed that which is compatible with the F-22 module. The Bendix connector was chosen for the same reason--namely it is the dominant connector being used on LFT modules at this time. The VMS modules are conduction cooled to air cooled racks because they are required to function even if the liquid cooling system fails. Being in air cooled racks, they are not dependent on the liquid cooling system.

Further trades will be performed to determine the optimum blend of COTS, affordability, and reliability. Technical issues to be investigated include connector, space and height for on-module DC to DC converters, commercial MCM compatibility, and I/O.

Arguments for other form factors include:

1) A larger board size would reduce cost because fewer boards would be needed. Less total "housekeeping" and interconnect circuitry would be needed for the total aircraft, since the "housekeeping" and interconnect circuitry is needed only on a per board basis.

2) The VME form factor should be considered because it is widely used and cheaper than the SEM-E form factor. It also has the advantage of being larger.

3) A new form factor should be designed which allows for ease of manufacture. This new form factor would be designed specifically for production on commercial manufacturing lines such as those used in the automotive industry.

3.7 Advanced Stores Management/Weapon System Interface

Standard:	Weapons System Interface
Goal:	To have an aircraft to weapon system interface standard which will be used by most future weapons in 2000 time frame.
Leading Candidate:	Mil 1760 Weapon Bus
Other Candidates:	Unified avionics network as a high speed addition to 1760, custom interconnects
Decision Date:	March 1996

The JAST weapons interface is proposed to be the F-22 Stores Management System (SMS) as implemented by MIL-STD-1760, Class II (except for Type B signals) with the possible enhancement of a higher speed channel. The functions performed by the SMS are: (1) store inventory, (2) missile monitor and control, (3) gun control, (4) expendable countermeasures (EXCM), (5) weapon bay door and launcher control, (6) selective and emergency jettison, and (7) BIT.

The JAST program is examining technology for carrying stores externally which will affect the weapons interface. These stores may include smart weapons with high-data-rate sensors or mission reconfigurable pods--also potentially carrying high-data-rate sensors. Of particular interest are those involving Global Positioning System (GPS) interfaces, video, and ATR processing. To accommodate these it may be necessary to augment the weapons system interface with a higher speed data link. If this is necessary, it is proposed to extend the unified avionics interconnect into the weapons system interface.

3.8 Advanced System Instrumentation and Software Debug Facility

Standard:	System Instrumentation and Software Debug Facility
Goal:	To establish a highly capable standard instrumentation and debug capability across all avionics.
Leading Candidate:	IEEE 896.5, Standard for Futurebus+, Profile M (Military), Annex A1, Software Development Unit.
Other Candidates:	F-22 system instrumentation and software debug facility
Decisions:	

As avionics architectures become more extensive and critical events affecting system behavior become separated by sub-microsecond times, the difficulty of integrating and maintaining the system is also increased in required sophistication. Various techniques, including real time non-intrusive (RTNI) monitoring have been developed to address these needs at the level of individual processors. However, it has been much more difficult to implement RTNI monitoring across an entire aircraft avionics system consisting of many processors. This section addresses the strategy to assure that all aspects of system monitoring, debug, and management remain within manageable bounds for the entire architecture.

The F-22 debug and instrumentation facility was the starting point for the JAST debug and instrumentation facility. However, additional features were deemed necessary for JAST. The following two paragraphs describe the F-22 features. These features were included as proposed functionality for JAST, not as a proposed implementation basis.

The F-22 Common Integrated Processor (CIP) architecture, hardware and software, provide the capability for the following debug and instrumentation functionality. The CIP provides two types of debug capability: low intrusive and intrusive (full debug capability). Both capabilities communicate with the VAX through the DRQ3B (DEC bus) and the CIP TM Bus (JIAWG standard bus for test and maintenance). These debug capabilities provide the application developers the capability to set breakpoints, halt processing, dump registers and memory, etc. The difference between intrusive and low intrusive debug is the type of debug commands provided to the developer (i.e. low intrusive debug allows instruction trace, low intrusive traps causes action, i.e. stop or dump register/memory (small)), while intrusive allows breakpoints, dumping of memory, etc.). The low intrusive debug function is supported only by the software in the operating system, while the intrusive debug function is supported by the software in the operating system and a separate software item, Debug Support Program (DSP). The debugging is used only during laboratory operations, not flight testing (normal operation).

The CIP also provides instrumentation for operation in the laboratory and flight test. This capability is provided with the aid of hardware and software components. The software components are the Simulation, Instrumentation and Debug Support (SIDS) and Data Pump (part of UFO (Utilities for Operational Flight Programs)). The SIDS software is located in the User Console Interface (UCIF) Module, while the Data Pump software is linked with each application that requires data to be pumped. The SIDS software commands the data pump software over the PI-Bus when to pump data (activation table) and what data to pump (definition table). These tables are built by the application developers before flight or laboratory run. The data is pumped across the PI-Bus and onto the fiber optic bus to the Data Acquisition Unit (DAU).

While the F-22 debug and instrumentation system is extensive, additional features were added for JAST. In particular, the system was enhanced to work across many processors. JAST supports a full hardware/software system test architecture as a subsystem on each smart (CPU based) module--system wide. The capability is in accordance with IEEE 896.5 Annex A. IEEE 896.5 Annex A provides a multi-processor instrumentation/ debug capability. It uses three very low latency discretes to trigger system wide watchpoint/breakpoint stop/start/halt etc. capabilities. High speed traces and dumps are implemented over a system instrumentation bus which requires a bandwidth per module cluster of at least 10 Mbit/sec. For the JAST architecture, the unified avionics network, SCI, is used.

During operational use, the application requires access to resource utilization measurements consistent with IEEE P1003.4bD8 "POSIX System Application Program Interface Amendment x: Real-time Extension". Specifically, interfaces described in Section 20 on Execution Time Monitoring should be supported non-intrusively so that dynamic load leveling may be accomplished as needed by the applications. Other measurements supported by IEEE 896.5 Annex A are also supported by application system calls (interrupt rates, I/O rates, qualified application execution timing (with or without interrupt, I/O, sub task overhead, etc.)).

3.9 Advanced Processors

Current core processor capabilities, such as used in the F-22, provide robust data and signal processing performance in common modular format. These capabilities, as noted in Annex A, are functionally divided, due to fault containment needs as well as the physical limitations of the electrical PI-Bus. The current methodology of clustering functions (Radar, EW, CNI) contains general purpose data, signal and graphics processing modules, but also a proliferation of special-purpose signal processing modules. Future mission requirements suggest a three times increase in processing throughput capability over the current F-22 mission requirements, primarily due to additional functions required in the Air-to-Surface missions and by timely advances in threat defense systems. These operational requirements have the great impact in avionics, all demanding significant increases in digital processing capabilities. In addition, advances in the sensor technology area demand higher performance processing with high utilization rates. The avionics architecture of an advanced strike aircraft should be scalable to allow addition of any, or all, of these additional functions. While the use of off-board sensors may reduce front-end signal processing needs, there will still be a significant processing load integrating the off-board data with on-board sensor data. An enhanced core processor for JAST should also support easy modification of functional capability through the addition/subtraction of common modules.

To make this flexible capability realistic and affordable, a number of enhancements over current systems are needed. First, a standard high performance (but simplified) unified network is needed. The use of such a network will alleviate data transfer bottlenecks at the backplane. A unified data distribution network which integrates FOTR/HSDB/DN functions (at a minimum) greatly simplifies system interconnect, lowers costs, improves reliability, and will remove physical limitations. The distance insensitivity of links of interconnects such as SCI allow for a "distributed backplane". With a distributed backplane, modules can be placed anywhere in the aircraft without having the bridge delay that exists today. Affordability trades will determine the need for the unified network to assume Test/Maintenance (TM) and PI Bus functions.

The second enhancement to current core approaches is to tightly couple within-processor module groups or clusters, which in turn are loosely coupled with other clusters. Current processing provides block data transfer capabilities for module-to-module data transfer, which is a midpoint between tight and loose coupling. The tight coupling for processor module-to-module communications increases the shared memory possibilities. Tightly coupled shared memory allows use of commercial parallel processor technology and simplifies software allowing it to be more scalable along with the hardware. Loose coupling of cluster-to-cluster communications provides for natural fault containment and security regions, as well as improved latency and simplification of software development (functions such as radar and EW can be developed independently except where integration and resource sharing is desirable).

The third key area for core processing enhancements is in the reduction of application-specific processing modules This will provide critical scalability and flexibility while increasing affordability in many areas. By reducing the number of unique module types and creating a more open architecture through the implementation of the unified network and other COTS elements, physical and functional boundaries are removed. Functions achieve a broader mapping across the architecture, reconfiguration options are increased, and a lengthened prioritized graceful degradation period is possible. Supportability is facilitated from the beginning to the end of the life cycle. System and software engineering environments are simplified, as fewer unique tools are required to support a reduced module set over the life of the system. System control and application inter-communication are improved. A larger purchase quantity of fewer module types will result in a reduced cost per module. Fewer module types reduces spare sets required on the flightline, enhancing availability while lowering logistics costs, and supporting two-level maintenance. Although further integration of the core processing is possible, affordability trades are needed to the its practicality. All phases of the life cycle cost will be impacted by these enhancements.

There are continuing trends in the commercial computing and microelectronics industry that will assist the core processing in making such enhancements to meet the requirements of future applications. COTS designs are certainly applicable in many cases. COTS components can be effectively employed to make avionics

supercomputing modules more affordable. A careful analysis of the degree of COTS influence will likely yield that its greatest impact will be at the device level, not the board level. Board level COTS components are not designed for the rugged environment of military avionics, but a combination of device level COTS components such as processing elements, memories, and interfaces with militarized packaging will yield very cost effective avionics supercomputing.

The utilization of COTS elements which allow the greatest degree of transparency in moving from development environments to the actual embedded avionics environment will provide the most cost effective computing solution. The goal in going from a development environment to the embedded environment is zero modification to the application software. This will provide dramatic reductions in EMD costs, and facilitate the reuse of hardware and software components between commercial and military avionics.

Parallel with commercial gains in processor technology, the electronics industry has developed unique methods and technologies for packaging such advanced devices for harsh operating environments, while maintaining architectural integrity, reducing interconnect levels and other key causes for failure. Such advancements in modular packaging will be vital to reducing EMD cost and meeting reliability, maintainability, and affordability (RM&A) requirements when integrating COTS components.

These enhancements to the processing hardware require concomitant changes in the software. Technologies such as real-time operating systems, software engineering environments, and compilers need to be further developed. The use of a standard application interface layer facilitates software reuse and transportability. Also, the commercial parallel processing compiler technology should be leveraged. The issues of software reuse and scalability are equally as important as the hardware when addressing overall reductions in LCC.

4.0 Software Design, Development, and Support

4.1 Introduction

The JAST avionics software architecture emphasizes affordability. Affordability is supported by a software architecture that is modular, supports open system standards, and can be tailored for a variety of missions and hardware architectures. The following sections describe the software architecture's features in detail.

4.2 Ada Programming Language

Standard:	High Order Programming Language Mil/ISO /ANSI 1815(x)
Goal:	A language designed for implementary large complex real time systems development. Supports quality software engineering practices.
Leading Candidate:	Ada 9x
Other Candidates:	Ada 83, C/C++, FORTRAN
Decision Date:	March 1996

Ada is the programming language of choice for the JAST avionics. In addition, ADA is required by public law, although exceptions are possible. The Ada programming language is an approved ANSI/MIL standard (1983) and an International Standards Organization (ISO) standard (1987). The current version of Ada, Ada 83, is under revision in accordance with ANSI and ISO procedures. Pending final standard approval, the revised Ada programming language is referred to as Ada 9x.

JAST avionics software will benefit in terms of reduced development costs, increased supportability, and improved software engineering methods by using Ada 9x. Ada 9x will provide explicit support for object-oriented programming (if desired), programming in the large, and real-time/parallel programming.

Ada 9x offers significant cost reductions for JAST avionics software. Ada 9x has specifically addressed issues concerning "programming in the large." First it offers separate compilation facilities. Ada 9x enforces full and strong type checking across separately compiled units of the application. A "library unit" is the basic independently compilable unit of an application. These library units may be organized in a hierarchical form. Note, this feature explicitly supports the JAST mission software architecture described in Section 4.1.3. The Ada 9x hierarchical library structure allows large software applications, such as the JAST avionics, to be organized into a set of functions, each composed of a tree of library units (JAST subfunctions).

The hierarchical Ada 9x library support offers areas for considerable cost reductions. When a JAST function and/or subfunction needs to be extended to support additional requirements, additional "child" library units can be added. This approach eliminates the need to edit existing library units, thereby avoiding the need to perform a complete software recompilation. Compilations for large systems consume massive amounts of time, often taking several days for a complete compilation and linking. Development time and costs can be reduced with hierarchical libraries.

4.3 Partitioned Avionics Software Architecture

The JAST avionics software is divided into two main partitions: Mission software and System/Support Software. The partitioning of the avionics software is specifically supported by the Ada 9x Programming Language (Section 4.4). In addition, partitioning allows for the affordable development of the JAST software. For example, an operational software system can be constructed from existing avionics software, commercial-off-the-shelf (COTS) software, and developed software. By adhering to strict partitioning and modularity guidelines the avionics software can be integrated into a working system (see Figure 4.3-1)

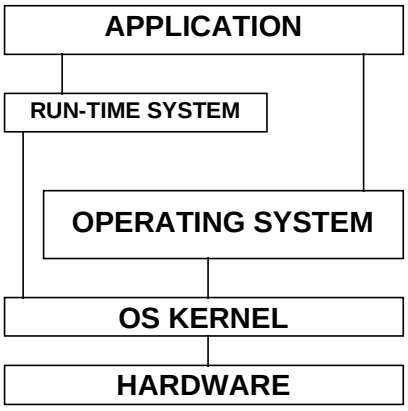

Figure 4.3-1 Generic Avionics Software Architecture

4.3.1 Mission Software

The JAST mission software is software that performs a function that needs to be under the pilot's direct control. In addition, mission software directly influences mission accomplishment. Finally, one can view the mission software as describing how the avionics system will act for a given mission. Several of the major mission software types are discussed below.

The JAST controls and displays software architecture allow for modifications to the information displayed on the multi-function displays by changing data and not lines of code. This data-driven approach provides a flexible and affordable methodology for implementing the JAST controls and displays. Control and display software can be implemented to the level of detail determined by the available software budget. Software that implements the graphics symbology should adhere to commercial graphics standards, graphic libraries, and support software to avoid the dependence on specialized graphic hardware interfaces. This approach defines an affordable mechanism for incrementally creating JAST symbology as new requirements emerge and more money becomes available.

The JAST master - mode - default software architecture allows for the definition of the default settings for all strike weapon system components. The master - mode - default software defines the location of cockpit displays, default sensor settings, standard electronic combat settings, radar modes, and Communication, Navigation, and Identification (CNI) defaults. This approach allows for the affordable addition and reconfiguration of JAST avionics initial conditions.

The JAST weapons delivery architecture software provides the ability to add or remove strike weapons from the aircraft stores management system. Affordability is emphasized by the capability to modify and/or add weapon flyout models, delivery parameters, missile launch envelopes, and safe escape constants. In addition, the capability to rapidly change weapon parametrics based on experience and testing will reduce software costs after flight testing.

The JAST mission planning software architecture allows for radar cross section management, flight planning, route optimization, fuel consumption computations, and time to climb/descend calculations. This software can be changed in an affordable manner by the weapon system user.

The JAST sensor management software architecture allows for the settings of sensor search volumes, sensor search patterns, and the definition of what sensor information is to be recorded. Affordability is emphasized by explicitly allowing the weapon system user (rather than software programmers) to define/change sensor management rules. This reduces development costs by avoiding the need to develop specific software for each pre-defined sensor management rule.

The JAST electronic countermeasures (ECM) software architecture allows the weapon system user to define and implement specific countermeasure techniques. Development costs are reduced by allowing the most recent techniques to be set (through software) once the weapon system is delivered.

4.3.2 System/Support Software

The system/support software provides mechanisms for controlling the execution of the avionics software and the management of mission essential data. Rather than describe how the avionics software acts, the system/support software emphasizes the structure and specific software execution for a particular instant in time. Some of the major system/support software types are discussed below.

The JAST avionics software architecture provides for control by the avionics operating system and run-time system (RTS). The major operating system goal is to maintain a partition between the hardware and software that minimizes disruptions when one partition undergoes a modification. For example, the JAST operating system will provide a set of interfaces to the avionics application software, i.e. an application program interface (API). The operating system interface also provides real-time data communication and control mechanisms that are independent of the underlying hardware implementation. In this way, the hardware dependencies are encapsulated within the implementation of the operating and RTS.

4.3.2.1 Application to Operating System Standard

Standard:	Portable Operating System Interface X(Unix) POSIX IEEE 1003
Goal:	Isolate application software from underlying processor hardware with standard interface. Provide services that every computer program needs such as I/O and program execution control.
Leading Candidate:	Portable Operating System Interface X(Unix) POSIX IEEE 1003
Other Candidates:	F-22 Operating System Custom O/S Kernel
Decision Date:	1st Qtr FY 98

The proposed operating system approach chosen for the JAST avionics software emphasizes affordability. First, the need for the development of a specialized operating system is proposed to be reduced by relying on the available features of the Ada run-time system and the real-time annex of POSIX. Second, the learning curve for programmers should be reduced. Programmers do not have to learn a new operating system to program JAST avionics software. Third, relying on standard operating system interfaces means that these interfaces are more likely to be bug free, thus avoiding costly corrections.

Ada 9x provides explicit features for low-level, real-time, embedded, and distributed systems such as the JAST avionics. These features are described in detail in the "Ada 9x Systems Programming Annex" (Annex G) and the "Real-time Annex" (Annex H). The specific features in these two Annexes allow the JAST avionics software readily available features that are needed for avionics software development.

The JAST avionics software will have access to interrupt support mechanisms via Ada 9x's Annex G. Compiler directives (pragmas) are provided for the designation of procedures to act as interrupt handlers. This allows interrupt handlers to be programmed in Ada without the need for programmers to have prior knowledge of a particular proprietary operating system's interrupt handling capability. Annex G also provides support for shared variable control. Once again, these built-in language features minimize the use of proprietary or non-open operating system services.

Ada 9x's Real-time Annex, Annex H, requires the System Programming Annex for support. Annex H consists mostly of documentation requirements. Specifically, an Ada 9x implementation must document the values of the annex-defined metrics for at least one hardware or system configuration. This information is necessary to ensure that the JAST avionics software can execute within the real-time constraints designated during the software design and specification phase.

The JAST avionics software will rely on the Ada 9x's tasking model. Ada 9x provides protective types. This allows for an efficient implementation of shared data access. Semaphores and other low-level primitive operations will now operate faster and safer than unstructured primitives.

4.3.2.3 Graphics Interface

Standard:	Graphics Interface
Goal:	Isolate application from graphics display hardware and to use tools and extensive graphics libraries available as COTS.
Leading Candidate:	X-11/Motif
Other Candidates:	PHIGS, GKS, Custom, F-22
Decision Date:	March 1996

4.3.2.4 Data Management

Data Management will be provided by a data manager program using Ada 9x and POSIX. Affordability is a major criteria in determining the functionality of an integrated data manager. In addition, the data manager must offer the necessary security mechanisms for protecting sensitive data.

4.3.2.5 Software Fault Tolerance

The JAST avionics software architecture provides the capability to detect, compensate, and correct for software faults. Fault-tolerance is provided through a combination of Ada language features, operating system mechanisms, and application code that ensure the integrity of the mission data.

4.3.2.6 Security

Security mechanisms for protecting software data and programs are planned to be provided by the operating system. Layered security features in the operating system separate operating system and other privilege states from ordinary application states. For example, several POSIX-compliant, secure operating systems provide layered security. In addition, a security mechanism within an operating system provides the capability to assign security labels to portions of memory. Software security can be enhanced with availability of hardware-based security implementations.

4.4 Mission Software Architecture

A representative avionics mission software architecture is described below. In this example, Ada's support for structured design and code helps in generating the software design from the overall avionics design.

The mission software architecture is a hierarchy of elements that implement avionics mission functions. The hierarchy is based on a functional decomposition starting with the avionics mission. The elements from the functional decomposition map to a corresponding Ada 9x structure. Further details of the software can be found by descending to a lower level in the hierarchy. The hierarchies are illustrated below.

- Avionics Mission => Mission Action Object
- Avionics Meta function => Distributed Cooperative Ada Partitions
- Avionics Function => Ada Library Unit
- Avionics Subfunction => Ada Package
- Avionics Requirement => Ada task/function/procedure

At the topmost level of the functional hierarchy is the avionics mission. The avionics mission is simply the combat task given to the weapon system. For example, JAST may lead to weapon systems that must conduct deep

air interdiction missions. The mission is described in terms of weapon system actions and operational profiles (i.e., altitude, target range, etc).

Metafunctions represent a characteristic action to be accomplished by a high level system element. Metafunctions are decomposed into functions used to define functional areas in greater detail. Functions in turn are further divided into subfunctions which define specific operations to be performed. Under subfunctions are requirements, which define specific activities that the subfunction must complete.

The Ada mission software architecture implements the avionics functional decomposition. The Ada software is defined by a mission action object. The mission action object is based on the scripts structure which describes a stereotyped sequence of events within a particular context. The mission action object maps to a set of distributed cooperative Ada partitions. The Ada partitions consist of a group of Ada packages. The Ada packages contain the particular tasks, functions and procedures.

There are many advantages to this particular architecture for the mission software. First and foremost is affordability. Avionics designers currently design the software and perform the avionics functional decomposition. A redundant effort by programmers is avoided. Second, the software architecture is explicitly supported by the Ada programming language. The Ada programming language, as described in Section 4.1.4, allows for the affordable development of large scale software systems. Third, the mission software architecture maps to the actions and results for a particular avionics mission. Weapon system users have direct visibility into the software. In addition, this mission mapping allows for the modular assembly and reconfiguration of software for each mission.

4.5 Software Development Process

The JAST software development process is a subset of the systems engineering process. Through the use of domain engineering and the analysis of F-18 and F-22 as examples of strike fighters, a reference software architecture is developed. This architecture will be refined by the JAST strike fighter requirements. The software will be developed using object oriented uniform principles and mapped to the software architecture. The software process is based on the Evolutionary Spiral Model. This process builds software in incremental steps adding detail and requirements at each step. By rapidly prototyping, modeling, and simulating the requirements are validated early, performance can be evaluated and the architecture refined as the software is developed. This process also encourages the reuse of software objects from contractor libraries, publicly available libraries, and selected objects from other strike aircraft.

4.6 Software Development Environment

The JAST avionics software development environment is built upon an approach described as domain specific software engineering. A domain is the functional area covered by a set of systems (e.g. avionics systems) where similar software requirements exist. Domain engineering is the process of developing a solution to a problem characterized by the domain. (See Figure 4.5-1.) The ultimate goal of the JAST SEE is to allow avionics software engineers the ability to use graphical design notations and advanced software tools to rapidly specify, simulate, and develop avionics software. Before a single line of code is written, avionics designers can be confident that the software design will satisfy cost, performance, and supportability goals. This approach offers significant cost savings in software development since the cost of changing the avionics software rapidly increases the further into the life cycle one progresses.

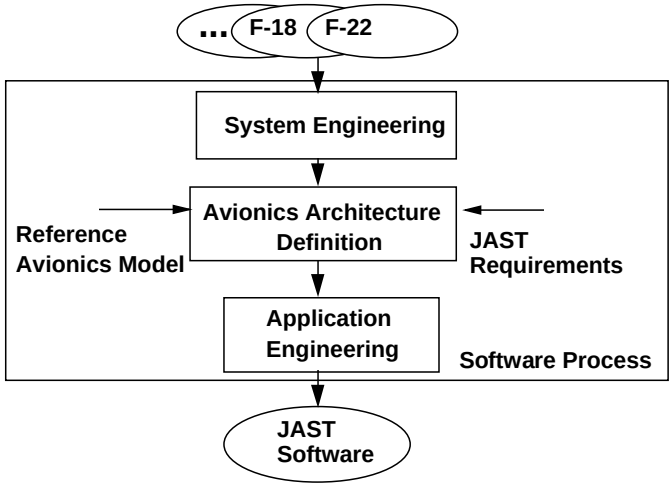

Figure 4.5-1 Domain Software Engineering

The JAST SEE focuses on solving the complex problem of creating an avionics system for conducting strike warfare. The JAST SEE supports the decomposition of the problem, specification of applicable solutions, the testing and analysis of the solutions, and the generation of avionics software that implement the solutions. The avionics software is generated through a combination of automatic programming, software component reuse, and a limited amount of manual coding.

Overall, domain specific software engineering results in development cost savings by reducing the labor costs involved in writing software. Emphasis on early testing and simulation of the software avionics solution and the minimization of manual programming saves time and labor costs.

4.7 Reuse

Software reuse is more than the just reusing software code. Software reuse also includes the reuse of software designs, specifications, and test program sets. There are five phases of software reuse: (1) Creation, (2) Preservation, (3) Retrieval, (4) Comprehension, and (5) Modification. Therefore, software reuse requires a SEE that supports these five phases. Specifically, the JAST SEE will need mechanisms for developing avionics software from reusing software components. However, for reuse to be successful for JAST, the software needs to be used at least once! A significant amount of software will be available for reuse by the EMD phase from the several planned JAST integrated demos. In addition, avionics software from other avionics programs (e.g., F-22) may be available for reuse.

Development cost savings may be realized by reusing avionics software. First, JAST can avoid the costs of developing software from scratch. Software can be assembled from components that include many lines of code rather than from individual lines of code. Second, existing designs, and specifications can be modified for use by JAST. Money spent on original design can be minimized. Third, if previously used and tested software is reused, software testing costs can be reduced during the development phase.

4.8 Information Architecture Concept

The concept of an information architecture is relevant to the JAST avionics system. The Air Force Science Advisory Board (SAB) sponsored a 1993 summer study on Information Architecture. It recommended that the Air Force develop an enterprise-wide information architecture. This was characterized as an enterprise-wide building code that is layered, open, and driven by COTS considerations. A focus on common data element definitions and on applications interface standards and conventions was also recommended. A process for managing architecture development was advocated as a means to apply an information architecture to both administrative corporate information management (CIM) applications and to tactical warfare (mission critical) applications. Three facets of this process apply to implementation of any information architecture. These facets are:

(a) Establishing a continuous process for evolving the "building code" to meet changing needs including opportunity with external organizations.
(b) Involving users and developers in assessing and evolving this building code.
(c) Applying with accountability the concept of "central direction and decentralized execution" to the architecture development process.

The architecture-driven system characteristics which result from this process are:

- Open systems - publicly known interfaces with wide vendor support
- Layered protocols - hierarchical system of well defined services that hides low-level functionality
- Common network services - consistent interface to and service from otherwise heterogeneous networks
- Common user services - widely usable network-based application and user support functions
- Extensibility - ability to incorporate new media and functions and to adapt to growing user population
- User interface tools - tools that facilitate the rapid construction of user interfaces
- Common security architecture - a common, consistent security policy, services, and implementation mechanism
- Priority, preemption - means to assure or deny system resources
- Domain-specific architecture - specialized information architectures using and supporting common characteristics of any application domain
- Applications interoperability - the direct exchange of information between different applications programs
- Common data dictionary - assures the consistent meaning and form of commonly transferred data and information elements
- Compatible analysis tools - user/operator programs that verify or evaluate architecture characteristics.

This concept is described in the following reference:

Druffel, L.D., et al, "Information Architecture Concepts to Support Air Force Anywhere, Anytime Mission Scenario," (a report of the 1993 Air Force Science Advisory Board (SAB) study on information architecture) in Proceedings of the American Defense Preparedness Association (ADPA) Conference on Battle Management Command, Control, Communications and Intelligence (C3I), USAFA , Colorado Springs, CO, March 23-25 1994.

The JAST Avionics architecture incorporates the information architecture in terms of both processes and products:

- Processes - system development programs which implement the architecture shall establish environments and methodologies for hardware and software design that incorporate the principles listed above.
- Products - the building blocks of the JAST avionics concept shall conform to the architecture - driven characteristics listed above.

5.0 Subsystem Architectures

5.1 Integrated RF Sensor System

The JAST program goal is to have fully integrated RF support equipment (IRSE);however, technology maturity, cost, and risk will dictate the amount of IRSE that will be appropriate for an EMD aircraft. Figure B.6-1 (in Appendix B) shows a top-level version of the IRSE. This section describes potential IRSE architectural standards which are candidates for a JAST avionics suite and also describes the avionics system architectural impact of the ISS concept which is the current leading candidate for the RF sensing function.

Referring to Figure B.6.1, note that aircraft-dependent RF apertures are interconnected to receive and transmit RF switches. Any number and types of antennas could be interconnected by the aircraft "custom" RF switch. Further, the RF switch might be configured as a single unit or distributed around the aircraft to accommodate remote sensors in the wings and/or tail. The near-term approach to implementing the RF network and switch is to use coaxial cables and strip-line type switches. In the future, analog photonics is expected to be used to replace this electrical network, with the expectation of reducing cost, weight, and EMI effects.

From the figure, it can be seen that a family of frequency conversion modules that span a specific RF bandwidth are used to either downshift RF to Immediate Frequency (IF) (receive) or upshift IF to RF (transmit). The number and type of frequency converters is a function of the maturity of the MMIC technology and the interface between the RF switch and the frequency converters is expected to change with the advent of analog photonics. Therefore, standards impacting the frequency conversion modules are not defined at this time. The family of IF modules will also undergo dramatic change because of progress in MMIC, miniature filters, acousto-optic devices and analog-to-digital (A/D) conversion technology. With the advent of these advancements, it is expected that the number of module types (and number of modules) will be substantially reduced and that intramodule interfaces will be simplified. Accordingly, this is a second area in which the establishment of standards at this time would be premature.

However, several other standards are potential candidates. For example, the use of SEM-E size modules will be continued as a standard for off-aperture RF support electronics. Also, a standard IF frequency plan will be adopted between the frequency converters and transmit/receive chain in order to promote hardware interchangeability and high volume production. Whether a separate IF frequency for High Dynamic Range (HDR) radar reception is needed to avoid spurious noise effects for high performance radars is a subject under current investigation. For low-cost radars having 60-70 dB dynamic range, a single IF frequency should suffice. Selection of a candidate standard IF frequency/frequencies will be made around 1996, with validation following in 1998.

Other candidate standards include the use of the unified network (e.g., SCI or SCI/RT) to control the network of RF modules, switches, and apertures. Also, a distributed electrical power standard and a RF/Digital connector standard will be defined by 1996. Liquid flow-through cooling of RF modules will be an established requirement before the first JAST aircraft is built. F-22 interfaces for liquid flow through cooling are the current baseline for JAST..

In the 2010 time frame, it is expected that analog, photonically-switched networks will support RF network communications, with IF modules having digitized front-ends. In general, radios will be the first RF functions to convert to digital since they have the least demanding A/D conversion requirements. The digital boundary is then expected to move towards the aperture (with the lower IF frequencies internal to the modules being digitized first) until digital radar and EW are achieved. With these strides in digital technology, separate pre-processors are expected to merge with the modules performing digital RF functions. Digital processing of RF-based contact fusion, processing of digital data-linked information, processing and control of low latency CNI and EW signals, digital control of both analog and digital modules, and a large portion of the IRSE Resource Management function is expected to be contained within the RF racks. The unified, likely in a photonically-switched configuration, and a photonic backplane with high bandwidth, low latency and low EMI signaling are candidate standards which will

be evaluated as the technology matures. Even further downstream, most RF signals will be digitized at the aperture and transmitted photonically to the RF rack. Packaging advances are needed to permit the close co-habitation of analog and digital signals. Although commercial MMIC micro-circuits may be used, it is not expected that the commercial marketplace will develop needed low-cost ceramic multi-chip packages needed for the fighter environment.

5.2 Radio Frequency Apertures

The JAST program goal is to have fully integrated RF apertures; however, technology maturity, cost, and risk will dictate to what degree this is achieved.

Complete platform RF aperture configurations based on two approaches are described in the next two sections. Each configuration addresses candidate RF functions for an advanced joint services strike aircraft. Functions span the 2 MHz to 18 GHz spectrum. Both the federated (current technology) baseline and the enhanced aperture configurations assume a fully functional IRSE "backend". The avionics system will be able to perform the following functions: Radar, EW, IFF, and CNI. The federated and enhanced (integrated) approached bracket the range within which the JAST architecture standard for RF apertures will be defined through analysis and demonstration of the alternatives.

5.2.1 Federated Aperture Configuration; Current Technology Baseline

The aperture configuration (by type, number of elements, band, and location) for an RF aperture suite based on current technology and other current technology apertures is shown in Table 5.2.1-1. In general, embedded antennas are assumed for low RCS. A skeletal depiction of the high-band (above 2 GHz) and directional functions above 0.5 GHz is shown in Figure 5.2.1-1. Omni antennas for UHF radio, Identification Friend or Foe (IFF) transpond, etc., are omitted for clarity. The main nose array for fire control radar functions is similar to current fighters. Four azimuth and two elevation situation awareness ESM arrays provide full RWR and directional finder (DF) capability from 0.5 to 18 GHz. The ECM apertures include 6 low band and 6 high band log-periodic apertures about the waterline of the aircraft. Two IFF arrays, one on each wing leading edge, provide forward IFF interrogate capability, like current technology. Two 2-to-18 GHz spirals fill in RWR coverage top and bottom. Two more 2-to-18 GHz spirals are used for ESM. Two small slot antennas provide MLS receive capability. Six small auxiliary active electronically scanned arrays (ESAs) (two bands) support two different data link functions. A horn or log-periodic spiral in front supports the carrier landing receive function. Also shown are the receiver low noise amplifier (LNA) and transmitter equipment required to interface the apertures to the IRSE. The aperture count for this configuration varies depending on the definition of an aperture. The total aperture count is 64 with each spiral in the 6 situation awareness arrays counted as an aperture.

Table 5.2.1-1 Notional Integrated RF Avionics Suite Based on JIAWG and Current Apertures

APER-TURE*	Function	TYPE **	#EL (EA)	BAND (GHZ)	LOCATION	FUNCTIONS
1	RADAR	AESA	2,000	8-12	FWD	RADAR, PASSIVE TARGETING
2-7	EW	SPIRAL	1	2-18	FWD-PORT, STBD AFT-PORT, STBD TOP/BOT	RADAR WARNING RECEIVER (RWR)
8-13	EW	LP	1	2-6	WATERLINE	ECM-(TRANSMITTER)TX
14-19	EW	LP	1	6-18	WATERLINE	ECM-TX
20-21	EW	SPIRAL	1	2-18	TOP/BOT	ECM-(RECEIVER) RX
22-33	EW	SPIRAL	1	2-18	6 PORT 6 STBD	SITUATION AWARENESS (SA), FWD SECTOR-TWO ARRAYS, EACH USES 1 RWR ELEMENT. AZ AND EL DIRECTIONAL FINDING (DF)
34-35	CNI	SLOT	1	5	FWD-BOT AFT-BOT	MICROWAVE LANDING SYSTEM (MLS)
38-43	EW	SPIRAL	1	0.5-2	4 PORT 4 STBD	SA, FWD SECTOR-TWO ARRAYS, EACH USES 1 RWR ELEMENT. AZ AND EL DF
44-45	CNI	LINEAR ARRAY	8	1-1.1	FWD-PORT, STBD	IFF INTERROGATE
46-47	CNI	SLOT	1	1-1.1	TOP/BOT	IFF TRANSPOND
48-49	CNI	SLOT	1	0.9-1.2	TOP/BOT	JTIDS/TACAN
50	CNI	SLOT	4	1.2-1.5	TOP	GPS
51-52	CNI	SLOT	1	0.2-0.4	TOP/BOT	UHF RADIO, HAVEQUICK
53	CNI	SLOT	2	0.1-0.33	BOT	ILS-GLIDESLOPE, LOCALIZER
54	CNI	SLOT	1	0.076	BOT	ILS-MARKER BEACON
55	CNI	SLOT	1	0.2-0.4	TOP	UHF SATCOM
56	CNI	LP	1	15	FWD-BOT	ACLS/PCSB
57-59	CNI	AESA	100	10	FWD-PORT WING FWD-STBD WING TAIL	COMMON HIGH BAND DATA LINK (CHBDL)
60-62	CNI	AESA	64	CLASSIFIED	TWD-PORT WING FWD-STBD WING TAIL	COOPERATIVE ENGAGEMENT CAPABILITY (CEC)
63-64	CNI	FERRITE	1	2-30	PORT/STBD	HF COMM, LINK 11

* Running total number of apertures

** Antenna types are notional

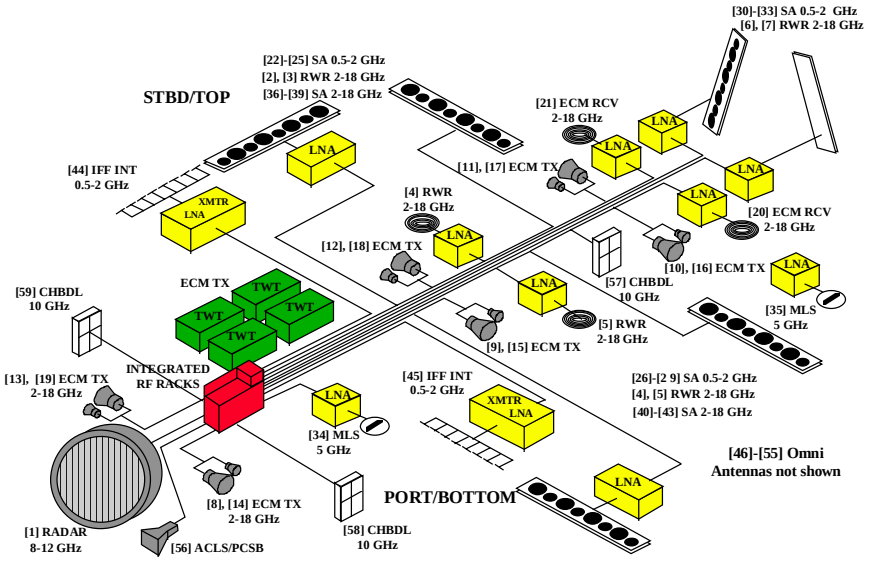

Figure 5.2.1-1 Notional Integrated RF Avionics Suite Based On JIAWG And Current Apertures (High Band And Directional Functions)

5.2.2 Enhanced Aperture Configuration

An enhanced aperture configuration based on shared apertures is shown in Figure 5.2.2-1. Table 5.2.2-1 identifies the shared functions each aperture provides. Three high band apertures are situated about the waterline of the aircraft. The main nose aperture performs fire control and other radar function in X or Ku-band. Other high band functions in the forward sector are performed by the main nose array. Two small auxiliary arrays fill in 360 degrees azimuth coverage. Three small active arrays provide 2-to-6 GHz coverage. One each is located on the leading edge of each wing with the third filling in AFT coverage. Two 2-to-18 GHz spirals fill in RWR and ESM functionality above and below the aircraft. Multi-arm spiral antennas (MASA) are used for functions in the 200 MHz to 2 GHz range. A total of 8 MASA are shared in this configuration, supporting the many functions in this frequency range, including threat warning and situation awareness. Multi-turn loop (MTL) antennas rely on excitation of structure in the airframe. Two antennas of one MTL type provide very high frequency (VHF) coverage and two of another type provide high frequency (HF) coverage. A total of 21 apertures may be required for this configuration. However, it must be noted that the total configuration of shared apertures especially looking below 2 Ghz must be refined.

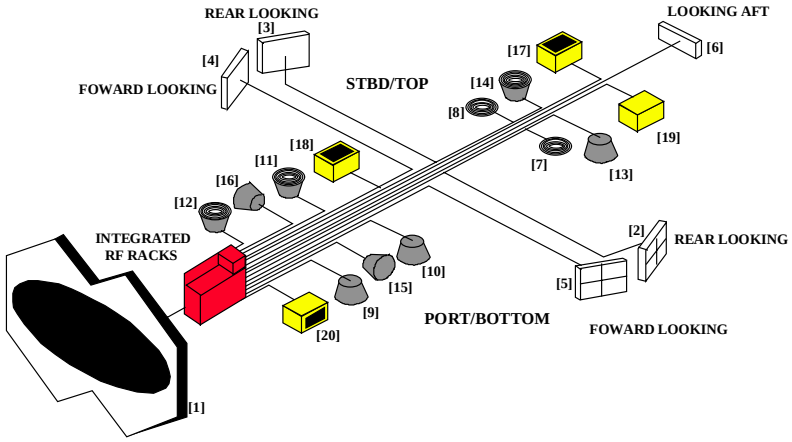

Figure 5.2.2-1 Notional RF Aperture Suite For Advanced Strike Aircraft Shared Approach

Table 5.2.2-1 Notional Integrated RF Avionics Suite Based On Shared Apertures

APER-TURE*	Function	TYPE **	#EL (EA)	BAND (GHZ)	LOCATION	FUNCTIONS
1	RADAR, EW, CNI	WBSA	3000	6-18	FWD	A/A & A/G RADAR, RWR, ECM, SA, PASSIVE TARGETING, CHBDL, ACLS, WEAPON DATA LINK
2-3	EW, CNI	WBSA	200	6-18	PORT WING-AFT STBD WING-AFT	RWR, ECM, SA, PASSIVE TARGETING, CHBDL
4-6	, EW, CNI	WBSA	64	2-6	PORT WING-FWD STBD WING-FWD TAIL-AFT	RWR, ECM, SA, DATA LINK, MLS
7-8	EW	SPIRAL	1	2-18	TOP/BOT	RWR, ECM RECEIVE
9-12	CNI	MASA	8-ARM	0.2-2	2 TOP 2 BOT	UHF RADIO, GPS, HAVEQUICK, AFSAT, GLIDESLOPE, JTIDS, TACAN, , IFF TRANSPOND /TCAS, ACMI (FUNCTIONS SPREAD AMONG 4 APERTURES TO MATCH COVERAGE AND FUNCTIONAL MIX)
13-14	CNI	MASA	8-ARM	0.2-2	TOP/BOT	IFF-INTERROGATE
15-16	RADAR, EW	MASA	8-ARM	0.2-2	PORT/STBD	RWR, SA, ECM, SAS
17-18	EW, CNI	MTL	1	0.03-0.2	TOP/TOP	VHF RADIO, SINCGARS, SELF PROTECT
19	EW, CNI	MTL	1	0.03-0.2	BOT	VOR, LOCALIZER, MARKER BEACON, SELF PROTECT, SINCGARS, VHF RADIO
20-21	CNI	MTL	1	0.002-0.03	PORT/STBD	HF COMM, LINK11

* Running total number of apertures
**Antennas types are notional

5.3 Integrated Electro-Optical Sensors

Electro-optical sensors are used for a variety of functions on tactical aircraft. The sensor configuration for an individual JAST platform may include any or all of the following functions:

- Targeting Forward Looking InfraRed (TFLIR) such as the AN/AAS-38 on the F/A-18 for identification and tracking of ground targets. Next generation TFLIRs will probably incorporate a large (640 x 480 or larger) staring mid wavelength focal plane array.

- Long wavelength InfraRed Search and Track (IRST) such as the AN/AAS-42 on the F-14D for autonomous and passive long range detection and tracking of air targets.

- Visible waveband television camera such as the AN/AXX-1 Television Camera Set (TCS) on the F-14 for visual identification of air targets.

- Laser Ranger/Designator (LRD) to support Laser Guided Bombs.

- Navigation FLIR (NFLIR) for pilotage, terrain following, and obstacle avoidance.

Additional functions to be considered include threat detection, situational awareness, and missile launch detection.

As with RF sensors, a range configurations from current federated designs to the JAST goal of a fully integrated EO sensor will be evaluated to define the JAST standard in this area. Functionally modular EO systems which can be tailored to fit the requirements of the platform. Combining integrated multi-function architecture with emerging technologies such as compact broadband optical systems, advanced focal plane arrays, and high speed digital signal processing will produce an affordable, smaller, lighter sensor suite with extended stand-off range and enhanced survivability. A single centralized installation makes it practical to equip low observable aircraft with a passive long range surveillance and targeting capability without compromising observability . In addition, a single conformal or semi-conformal window assembly should be less expensive to install and maintain than multiple large field-of-regard windows. The smaller size of the sensor suite also makes it practical to equip smaller aircraft (e.g. short takeoff and vertical landing) with targeting and surveillance capabilities thereby extending the benefits of EO systems to close air support operations.

As an example, an integrated Electro-Optical sensor architecture could combine a long range IRST with an advanced TFLIR and LRD behind a single semi-conformal window with an Advanced Distributed Aperture System (ADAS), an arrangement of low cost Mid Wave infrared (MWIR) starring arrays distributed around the aircraft. The IRST/TFLIR/LRD will provide precision targeting and long range target detection, while the ADAS provides situational awareness, missile warning, and navigation.

5.3.1 Processing Requirements

The following input and output channels are required for the Electro-optics architecture. The input channels will include the interface from the EO focal plane array to send intensity data to the signal processor; the interface between the mission data processor and the signal processor for mode changes, request for status command messages, and inertial navigation update messages; and the interface from the system mass memory for program download to the signal processor.

The output channels will include a data channel from the signal processor to control the sensor gimbals and stabilization; the output from the signal processor to the mission data processor of suspected target reports and status reports for the FLIR and track files after each frame update from the IRST; and the output on the video distribution network to the video display every frame update rate. This data represents pixel intensity that will be mapped onto the display format for the FLIR and track updates every scan bar for the IRST. Appendix E contains a summary of projected data rates associated with the RO sensing function.

The data rate projection for a 640 x 480 pixel FLIR operating at 30 frames per second is approximately 160 Mbits per second for 16 bit words. The rate will be scaled upward if a 1000 x 1000 pixel array is considered. The anticipated throughput projection is 3 - 10 GFLOPS.

The data rate and throughput calculations for an IRST are highly dependent on update rate, scan, resolution, and algorithm complexity. It should be assumed that spatial-temporal detection processing (500 - 1000 operations per pixel) will be used in the 2010 time frame. Depending on the scenario, the data rate is expected to be 120 - 200 Mbits/sec and the throughput 4 - 10 GFLOPS.

It will be assumed that the threat warning, navigation, and situational awareness functions will be handled by ADAS. For threat warning, ADAS acts as an array of IR detectors distributed throughout the airframe to detect missiles and aircraft at short range. A relatively simple algorithm should be adequate for this function. The data rate is expected to be about 500 Mbits/sec with a throughput projection of 1-2 GFLOPS.

Navigation produces a faster display that provides the pilot with an unobstructed view no matter which way he turns his head. Because of the multiple sensors involved, the data from each sensor must be merged to produce a

seamless image adding complexity to this function. The navigation data rate for ADAS can be as high as 2 Gbits/sec with a throughput projection of 1 - 2 GFLOPS. For a conventional NAVFLIR the data rate projection should be about 300 - 500 Mbits/sec for a 1000 x 1000 pixel array.

Situational awareness consists of detecting and tracking objects over the full field-of-regard. The complexity of the algorithms is comparable to the IRST, but over a larger field-of-regard. The data rate projection is 500 Mbits/sec and the throughput projection is 15 - 20 GFLOPS.

5.4 Off-Board Assets

The JAST program goal is exploring the use of off-board assets to reduce the cost and enhance the performance of next-generation strike aircraft. In the broadest context, off-board asset exploitation/utilization is herein defined to include all assets, sources of information or sensors, and strike-supporting functions that are or could be “off-board” to ownship airframe-based avionics. These off-board assets, therefore, range from the more traditional existing and potential in-theater spaceborne, airborne, and surface passive assets to in-theater active assets, and to sensors/avionics within actual weapons attached to and launched by ownship or pods attached to ownship. Given that these assets could be used effectively and reliably, this broad definition has significant impacts on the required types and capabilities of ownship avionics. Off-board asset exploitation/utilization can enhance situational awareness, especially beyond ownship sensor range, improve target and threat identification, provide information on time-critical targets, perform defensive functions for ownship, supporting flight mission replanning or modify air combat mission via updates, reduce or eliminate radiated emissions, and allow for launch of stand-off air-to-surface and air-to-air weapons beyond visual range.

Theater-based passive asset exploitation/utilization has also been referred to as Real-Time Information in the Cockpit (RTIC) and is defined as those system capabilities required to provide airborne aircrews timely and essential off-board information to allow mission adjustments in response to rapidly changing combat conditions. Currently, intelligence sources provide pre-mission planning support for all conventional aircraft mission roles. However, there is a limited in-flight capability to supplement or update information from pre-mission planning or onboard sensors. Current voice communications systems do not support high-volume, rapid data transfers, nor the passage of correlated data from multiple sources to adequately respond to changes in the operational environment. In addition, voice communications greatly increase aircrew workload. The RTIC concept envisions the capability to transmit accurate, timely, and consistent mission essential information to airborne aircraft worldwide and to augment onboard sensors. As such, this concept can serve as a force multiplier and enhancer for aerospace control, force application, and force enhancement roles.

Theater-based active asset utilization, e.g., escort jamming, stand-off jamming, combat air support, etc., can perform some defensive functions for ownship, although active end-game defense may still have to be done by ownship defensive avionics. Weapons or pods attached to ownship may have more sophisticated sensors and specialized processing than ownship avionics.

Exploiting and utilizing theater-based off-board assets will depend on these assets being in-theater with proper coordination and secure dissemination of the data and functions needed for support of ownship. Ownship avionics will benefit form the reduction or elimination of some sensors or other functions, but will require increased of digital communication sensors along with their waveform processing, increased core processing to filter and correlate/fuse this off-board data and/or perform the additional functions described above, and proper displays and controls and the associated processing that permits aircrew control, tailoring and detailed data access options.

In summary, several concepts are in the early formative stages, but there are operational and technical issues that need to be addressed in order to define and evaluate alternative options and concepts for off-board asset exploitation/utilization for highly maneuverable strike platforms

6.0 List of Leading Candidate Standards

The following documents are the standards and specifications which represent leading candidates for the "building codes" of the JAST Avionics system.

Digital Interconnect Standards:

- IEEE Std 1596-1992, IEEE Standard for Scalable Coherent Interface (SCI), Published by the Institute of Electrical and Electronics Engineers. (To be used until SCI/RT is available.)
- Draft IEEE 1596.6, SCI/RT Scalable Coherent Interface for Real Time Applications, Available via Internet. (Expected completion March 1995.)
- MIL-STD-1553B, Aircraft Internal Time Division Command/Response Multiplex Data Bus (May be used to connect to existing equipment that has 1553B interfaces.)

Weapons System Interface Specification:

- MIL-STD-1760

Module Mechanical Specifications:

- F-22 Line Replaceable Module Connector Specification, Rev A, December 1993, Document No. 5PTA3278
- F-22 Common Module Specification, June 1993, Document No. 5PTA3242

Cooling Specifications:

- Polyalphaolefin (PAO): MIL-C-87252, Coolant Fluids, Hydro-Lytically Stable, Di-electric, 2 Nov 1988,
- F-22 Common Module Specification, June 1993, Document No. 5PTA3242 (Specifies inlet temperature to the module of the cooling fluid.)

Pinout Specification:

- Planned Development by IEEE SCI/RT Working Group. Expected completion March 1995

Power Specification:

- Based on the power specifications given in the following: IEEE 896.5, IEEE Standard for Futurebus+, Profile M (Military), Section 6.4.1 Profile Power. IEEE 896.5 is available from the IEEE.

Backplane Discrete Specifications:

Based on the utility signals specification given in:

- IEEE 896.5, IEEE Standard for Futurebus+, Profile M (Military), Section 4.2.7 Utility Signals. IEEE 896.5 is available from the IEEE.
- J-89-N1, Rev C, JIAWG Utility Signals

Software High Level Language Standard:

- MIL/ANSI STD 1815A, Ada 9X

Operating System Standard:

- IEEE 1003-P1003, IEEE Standard for Information Technology - POSIX
- 1003.0 Guide to POSIX
- 1003.1 POSIX Systems Services & C Language Bindings
- 1003.4 Real-time Extensions
- 1003.5 Ada Bindings
- 1003.6 Security Extensions To POSIX
- 1003.13 Real-time Profiles
- 1003.18 POSIX Platform Environment Profile
- 1003.20 Real-time Ada Binding Profiles
- 1003.21 Real-time Distributed Systems

Graphics Standards:

- X Windows/ Motif
- GKS
- PHIGS

Processor Software and Hardware Instrumentation Standard

- Based on specifications given in the following: IEEE 896.5, Standard for Futurebus+, Profile M (Military), Annex A1, Software Development Unit. IEEE 896.5 is available from the IEEE.

List of Acronyms

A/A	Air-to-Air
AAST	Advanced Avionics Subsystems and Technologies
AAW	Anti-Air Warfare
ABI	Avionic Bus Interface
ACMI	Air Combat Maneuvering Instrumentation
ACP	Audio Control Panel
A/D	Analog to Digital
ADARS	Advanced Defensive Avionics Response Strategy
ADAS	Advanced Distributed Aperture System
ADM	Avionics Health and Maintenance Manager
AESA	Active Electronically Steerable Array
AFMC	Air Force Materiel Command
A/G	Air-to-Ground
Ai	Inherent Availability
AIMS	ATF Integrated Maintenance System
AFMSS	Air Force Mission Support System
AM	Amplitude Modulation
Ao	Operational Availability
AOA	Angle of Arrival
AOS	Avionics Operating System
API	Application Program Interface
APS	Array Power Supply
ARM	Anti-Radiation Missiles
ARPA	Advanced Research Project Agency
ASAP	Advanced Shared Aperture Program
ASDN	Aperture Signal Distribution Network
ASIC	Application Specific Integrated Circuit
ALSC	Adaptive Side Lobe Cancellation
ASM	Avionics System Manager
ASMD	ASM Distributed
ASMFM	ASM File Manager
ASML	ASM Linkable
ASMM	Avionics System Manager Master
ASMSC	ASM System Control
ASTOVL	Advanced Short Take-off and Vertical Landing
ATE	Automatic Test Equipment
ATF	Advanced Tactical Fighter
ATIMS	Airborne Tactical Information Management System
ATIP	Advanced Technology Integration & Prototyping
ATR	Automatic Target Recognize
ATS	Air-to-Surface
AVTR	Airborne Video Tape Recorder
BC	Bus Controller
BDA	Battle Damage Assessment
BIT	Built-In Test
BITE	Built-In Test Equipment
BIU	Bus Interface Unit
BSC	Beam Steering Computer
BSI	Backplane Signaling Interface
BUR	Bottom-Up Review

BVR	Beyond Visual Range
C^2	Command and Control
C^3I	Command, Control, Communications, and Intelligence
C^4I	Command, Control, Communications, Computer, and Intelligence
CAB	Common Avionics Baseline
C&D	Controls and Displays
CAG	Carrier Aircraft Group
CALS	Computer Aided Logistics Support
CASE	Computer Aided Software Engineering
CATS	Common Automated Test System
CC	Common Component
CCOK	Crypto-Checksum OK
CD-ROM	Compact Disk Read-Only Memory
CHBDL	Common High Band Data Link
CEC	Cooperative Engagement Capability
CID	CIP unit ID
CIP	Common Integrated Processor
CIS	Combat Intelligence System
CND	Cannot Duplicate
CNI	Communication, Navigation and Identification
COMSEC	Communications Security
COTS	Commercial Off-The-Shelf
CP	Core Processing
CPI	Coherent Processing Intervals
CPU	Central Processor Unit
CRC	Cyclic Redundancy Check
CRGM	Coarse Real Beam Group Map
CSCI	Computer Software Configuration Item
CSI	Common Standard Interface
CSR	Command and Status Registers
CSR	Control or Status Register
CW	Continuous Wave
D/A	Digital to Analog
DAU	Data Acquisition Unit
DC	Direct Current
DDPES	Dual Data Processing Element Server
DDS	Direct Digital Synthesis
DF	Direction Finding
DHM	Diagnostic Health and Maintenance
DMA	Direct Memory Access
DN	Data Network
DNP	Data Network Portal
DPES/1553	Data Processing Element Server/1553
DRF	Digital RF
DSP	Debug Support Program
DSPE	Dual Signal Processing Element
DTC	Data Transfer Cartridge
DTE/MM	Data Transfer Equipment/Mass Memory
DTI	Debug Trigger Interrupt
DTOCS	Data Transfer Operational Control Software

DTU	Data Transfer Unit
EA	Enhanced Architecture
EC	Electronic Combat
ECL	Emitter Coupled Logic
ECM	Electronic Countermeasures
ECCM	Electronic Counter-Countermeasures
ECS	Environmental Control System
ED	End Delimiter
EEPROM	Electronically Erasable Programmable Read Only Memory
EID	Extended ID
EMCON	Emissions Control
EMD	Engineering, Manufacturing & Development
EMI	Electro-Magnetic Interference
EO	Electro-Optical
EP	Electronic Protect
EPS	Electrical Power System
ERP	Effective Radiated Power
ES	Electronic Support
ESA	Electronically Scanned Array
ESM	Electronic Support Measures
EXCM	Expendable Countermeasures
EW	Electronic Warfare
F^2I	Form, Fit and Interface
F^3I	Form, Fit, Function and Interface
FADEC	Full Authority Digital Engine Controller
FCR	Fault Containment Region
FDDI	Fiber Distributed Data Interface
FDR	Flight Data Recorder
FE	Front End
FFT	Fast Fourier Transform
FIFO	First In, First Out
FIRM	Functionally Integrated Resource Manager
FIU	Fiber Interface Unit
FLEX	Force Level Evaluation
FLIR	Forward-Looking Infrared
FM	Frequency Modulation
FMEA	Failure Modes and Effects Analysis
FNIU	Fiber Network Interface Unit
FOTR	Fiber Optic Transmitter/Receiver
FOTX	Fiber Optic Transmitter
FOV	Field of View
FPA	Focal Plane Arrays
FRC	Functional Redundancy Checking
FRC	Failure Redundancy Check
FRGM	Fine Real Beam Group Map
GAP	GBM Application Port
GBM	Global Bulk Memory
GMTI	Ground Moving Target Indicator
GPVI	Graphics Processor and Video Interface
GPS	Global Positioning System

HAC	Hughes Aircraft Company
HARM	High Speed Anti-Radiation Missiles
HDR	High Dynamic Range
HF	High Frequency
HMD	Helmet Mounted Display
HOTAS	Hands-On Throttle and Stick
HPRF	High Pulse Repetition Frequency
HUD	Head-Up Display
HSDB	High Speed Data Bus
HSDBIF	High Speed Data Bus Interface
HWCI	Hardware Configuration Item
I	In-phase
IAR	Integrated Avionics Rack
IC	Integrated Circuit
ICP	Integrated Control Panel
ICP	Integrated Core Processor
ID	Identification
IDF	Interface Database File
IEEE	Institute of Electrical and Electronic Engineers
I/F	Interface
IF	Intermediate Frequency
IFDL	Intra-Flight Data Link
IFF	Identification Friend or Foe
ILS	Instrument Landing
INFOSEC	Information Security
INS	Inertial Navigation System
I/O	Input/Output
IOBD	Integrated On-Board Diagnostics
IOC	Initial Operational Capability
IPT	Integrated Product Team
IR	Infrared
IR&D	Independent Research and Development
IRS	Inertial Reference System
IRSE	Integrated RF Support Equipment
IRST	Infrared Search and Track
ISA	Instruction Set Architecture
ISAR	Inverse Synthetic Aperture Radar
ISO	International Standards Organziation
ISS	Integrated Sensor Suite
ISS	Integrated Sensor System
ITDs	Integrated Technology Demonstrations
IVSC	Integrated Vehicle Subsystem Control
JAST	Joint Advanced Strike Technology
JIAWG	Joint Integrated Avionics Working Group
JTAG	Joint Test Action Group
JTIDS	Joint Tactical Information Distribution System
KOV-5	Cryptographic processor designation
LADARs	Laser Detection and Ranging

LCC	Life Cycle Cost
LCD	Liquid Crystal Display
LFT	Liquid Flow Thru
LLSP	Low Latency Signal Processor
LNA	Low Noise Amplifier
LO	Low Observable
LOC	Lines of Code
LPI	Low Probability of Intercept
LPRF	Low Pulse Repetition Frequency
LRD	Laser Range Designator
LRM	Line Replaceable Module
LRU	Line Replaceable Unit
LVDS	Low Voltage Differential Signaling
MASA	Multi-Arm Spiral Antenna
MATT	Multi-mission Advanced Tactical Terminal
MAW	Missile Approach Warning
MBV	Model Based Vision
MC&G	Mapping, Charting, and Geodesy
MCM	Multi-Chip Module
MCOTS	Militarized COTS
MCT	Mean Corrective Time
MDT	Mean Down Time
MFD	Multi-Function Display
MFLOPS	Millions Floating Point Operations Per Second
MIDS/LTV	Multi-function Information Distribution System/Low Volume Terminal
MIL-STD	Military Standard
MIPS	Million Instructions Per Second
MJPB	Multi Job Parameter Block
MLD	Missile Launch Detection
MLS	Microwave Landing System
MM	Mass Memory
MM	Mission Management
MMC	Module Maintenance Controller
MMIC	Monolithic Microwave Integrated Circuit
MOPS	Million Fixed Point Operations Per Second
MR	Master Reset
MRF	Multi-Role Fighter
MS	Mission Software
MSS	Mission Support System
MSTS	Multi-Source Tactical System
MT	Monitor Terminal
MTBCF	Mean Time Between Critical Failure
MTBF	Mean Time Between Failure
MTL	Multi-Turn Loop
MTM	Module Test and Maintenance
MTTR	Mean Time To Repair
NATO	North Atlantic Treaty Organization
NCTI	Non-Cooperative Target Identification
NGCR	Next Generation Computer Resources
NIU	Network Interface Unit
NRF	Non-RF

NRSP	Non-RF Signal Processor
NSA	National Security Agency
NVG	Night Vision Goggles
NVM	Non-Volatile Memory
O&S	Operational and Support
OFP	Operational Flight Program
PAO	Polyalphaolefin
PC	Power Conditioner
PCB	Process Control Block
PCT	Privilege Control Table
PD	Pulse Doppler
PDC	Power Distribution Controller
PDI	Post Detection Integration
PDU	Protocol Data Unit
PDW	Pulse Descriptor Words
PE	Processing Element
PEO	Program Executive Officer
PGM	Precision Guided Munitions
PI	Parallel Interconnect
PI	Parallel Intermodule
PIS	Power Input Section
PIU	PI Bus Interface Unit
PLL	Phase-Locked Loop
PMA	Portable Maintenance Aid
PMFD	Primary Multi-Function Display
PMD	Portable Maintenance Drive
POD	Point of Departure
PRCB	Processor Control Block
PRI	Pulse Repetition Interval
PRF	Pulse Repetition Frequency
PVI	Pilot Vehicle Interface
PWB	Printed Wiring Board
Q	Quadrature
R&D	Research and Development
RAM	Random Access Memory
RAIU	Remote Aperture Interface Unit
RBGM	Real Beam Ground Map
RDT&E	Research, Development, Test & Evaluation
RF	Radio Frequency
RGHPRF	Range Gated High Pulse Repetition Frequency
RISC	Reduced Instruction Set Computer
RL	Rome Laboratory
RM&A	Reliability, Maintainability, & Affordability
ROC	Reliable Optical Connector
ROM	Read-Only Memory
RRD	Risk Reduction Demonstrations
RSE/RFR	Radar Support Electronics/RF Receiver
RSS	Runtime System Service
RT	Remote Terminal

RTIC	Real-Time Information in the Cockpit
RTNI	Real-Time Non-Intrusive
RTS	Run-Time System
RW	Radar Warning
RWR	Radar Warning Receiver
RX	Receiver
RVM	Reference Validation Mechanism
S&T	Science and Technology
SA	Situational Awareness
SAE	Service Acquisition Executive
SAE	Society of Automotive Engineers
SC	Software Component
SAR	Synthetic Aperture Radar
SASSY	Shared Aperture Sensor System
SATCOM	Satellite Communications
SCI	Scalable Coherent Interface
SCI/RT	Scalable Coherent Interface/Real Time
SD	Starter Delimiter
SDN	Sub-Data Network
SEAD	Suppression of Enemy Air Defense
SEE	Software Engineering Environment
SEL	Single Event Latch
SEM-E	Standard Electronic Module-Format E
SEPE	Sort Enhanced Processing Element
SIDS	Simulation, Instrumentation, and Debug Support
SIMAS	Survivable Integrated Multi-function Antenna System
SMFD	Secondary Multi-Function Display
SMS	Stores Management System
SP	Signal Processor
SP	Self-Protect
SPE	Signal Processing Element
SPEOS	Signal Processing Element Operating System
SRAM	Static Random Access Memory
S/SEE	Systems/Software Engineering Environment
SSIG	Standard Signal Interface Group
STW	Strike Warfare
SUROM	Start-Up Read Only Memory
TACAN	Tactical Air Navigation
TAD	Technology Availability Date
TCB	Trusted Computing Base
TCS	Television Camera Set
TF/TC	Terrain Follow/Terrain Clearance
TIBS	Tactical Information Broadcast Service
TM	Test and Maintenance
TMR	Triple Modular Redundant
TO	Technical Order
TOA	Time of Arrival
TOD	Time of Day
TPIPT	Technical Planning Integrated Product Team
T/R	Transmit Receive
TRAP	TRE and Associated Applications

TRE	Tactical Receive Equipment
TSD	Time Synchronization Discrete
TSMD	Time Stress Measurement Device
TX	Transmitter
U&S	Utilities and Subsystems
UCIF	User Console Interface
UHF	Ultra High Frequency
UFD	Up-Front Display
UFO	Utilities for Operational Flight Programs
UMP	UCIF Master Present
USD(A&T)	Under Secretary of Defense for Acquisition and Technology
VAP	Virtual Avionics Prototype
VGPO	Velocity Gate Pull Off
VHF	Very High Frequency
VHSON	Very High Speed Optical Network
VLSI	Very Large Scale Integration
VMS	Vehicle Management System
VR	Voltage Regulator
WDL	Weapon Data Link
WGS	World Geodetic System
WL	Wright Laboratory